Biographies

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Thomas Aichinger received his M.S. degree in physics from the Karl-Franzens University in Graz in May 2007. During his diploma thesis, concerning the implementation of Charge Pumping in the laboratory soft- and hardware environment, he was integrated in the Quality and Reliability group of Infineon Technologies Villach. Currently he is pursuing his doctor degree at Infineon Villach and KAI in cooperation with the "Christian Doppler Laboratory" group of the Institute for Microelectronics in Vienna. In 2007 he recieved the Best Paper arward at ESREF.

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Douglas Brisbin received his B.S. from Miami University, M.S. and Ph.D. in Physics from Kent State University. He joined National Semiconductor in 2001 and is currently working as Principal Device Reliability Engineer in the Advanced Process Technology Development group. His interests are in the area of MOS/bipolar hot-carrier degradation, ultra-thin gate oxide integrity and NBTI. He is an active member of the JEDEC 14.2 Wafer Level Reliability Standards Committee and contributed to more than twenty five technical publications.

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Patrick Casey graduated from the Dublin Institute of Technology in 2006 with a first class honours degree in Physics and Physics Technology. He was awarded a postgraduate research scholarship by the Irish Research Council for Science Engineering and Technology (IRCSET) in 2006 which was jointly funded by IRCSET and Intel Ireland. He is currently in the third year of his PhD research programme at Dublin City University studying the growth, stability and electrical characterisation of MgO thin films on silicon substrates.

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Anna Cavallini is Full Professor at the Faculty of Sciences of the University of Bologna. She is member of the International Scientific Committee of the conferences GADEST, BIAMS, DRIP, EDS and ICDS. She has been working on elemental and compound semiconductors by investigation of (i) transport properties, (ii) structural and electrical properties, (iii) bandgap electronic levels. Since '90 she has been involved in research on radiation detectors on GaAs, CdTe and CdZnTe, focusing her study on native and process-induced defects. She is presently very active on nanotechnology by studying nanoscale defects in new materials such as InN and multi-quantum-well devices.

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Andrea Cester received the master degree in Electronic Engineering on 1998 and the PhD in Electronic and Telecommunication Engineering on 2002 from the University of Padova (Italy). Since 2002 he joins the Information Engineering Department - University of Padova as Assistant Professor. His research interests cover: Reliability of organic semiconductor devices (OTFT, OLEDs and organic solar cells); hot electron degradation and ionising radiation effects of ultra-thin gate oxide, MOSFETs, and novel non-volatile memories (nanocrystal, ferroelectric, and phase- change memories); Electrostatic Discharge effects on CMOS devices breakdown and reliability. He is author of more than 100 papers in international journals and/or conferences.

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Fen Chen received his Master degree in Physics in 1994, and his Ph.D. degree in Electrical Engineering in 1998 from University of Delaware. From 1997 to 1998, he was with IBM System Group at Rochester, MN and Intel Component Research at Santa Clara, CA as a graduate intern working on system stress and IC interconnect reliability. He joined IBM microelectronics at Essex Junction, VT in 1998 and has worked on semiconductor technology reliability issues since that time. During the past several years he has focused on low-k ILD TDDB issue for various IBM and IBM Alliance development programs.

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Karim Cherkaoui obtained his Ph.D. in 1998 from the Institut National des Sciences Appliquées of Lyon, France. Since he joined the Tyndall National Institute (formerly NMRC) in 1999, he has established and developed low temperature spectroscopy techniques including Deep Level Transient Spectroscopy (DLTS). During this period he gained experience in the spectroscopy of defects in semiconductors and devices. Since 2003, he has been involved in the area of high dielectric constant materials for microelectronics applications. He participated in several European and Irish research projects.

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Dr. Kin P. Cheung, obtained a Ph.D. degree in physical chemistry from New York University in 1983. From 83 to 85 he was a post doc at Bell Laboratories during which he pioneered Terahertz Spectroscopy. From 1985 to 2001 he was a member of technical staff in Bell Laboratories at Murray Hill. From 2001 to 2006, He was an associate professor at Rutgers University. He is currently a project leader at the National Institute of Standards & Technology, Semiconductor Electronics Division. Dr. Cheung published over 110 refereed journal and conference papers. He authored a book on plasma charging damage, a book chapter, and edited three conference proceedings. He served as committee member in a number of international conferences and has been invited to give tutorials in 9 international conferences. His area of interest covers VLSI technology, including processing technologies such as metallization and etching. More recently, he has been working on technology integration, gate oxide reliability and device reliability. His current interests include, in addition to CMOS characterization and reliability, MEMS wafer level packaging, microwave spectroscopy self-assembled-monolayer and micro-plasma arrays.

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Luca Chiavarone was born in 1971. He received the PhD degree in Physics from the University of Bari, Italy, in 2000 with a thesis on the study of the optical properties of conjugated polymer thin films and the fabrication of electroluminescent organic devices. In 2000 he joined the Research and Development Department, STMicroelectronics, in the Non-Volatile Memory Process Development Group working at first on electric wafer sort and then on the characterization, reliability and multilevel applications of flash cells. On March 31st, 2008 he joined Numonyx where he is currently flash reliability expert. His research interests include flash memory physics, technology and reliability.

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Craig Child received a Ph.D. degree in Chemical Physics in 1996 from The University of Texas at Austin. From 1996 to 2001, he was with 3M Corporation in Austin, Tx working as a laser physicist in the Electronic Products Division. In 2001, he joined Intel Corporation in Hillsboro, OR as a backend of line integration engineer working on 130nm, 90nm, 65nm, and 45nm technology nodes. In 2007, Craig joined the IBM ASTA/ISDA alliance as an AMD employee working on ULK integration in the 45nm and 32nm technology nodes.

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Andrea Chimenton graduated in Electronic Engineering in 2000 with full marks and received the Ph.D. degree in Information Engineering in 2004 both at the University of Ferrara (Italy) where he joined the Engineering Department in 2002 as Assistant Professor. His research activity is mainly focused on electrical characterization, physical and statistical modeling and reliability assessment of Non-Volatile Memories such as NOR-Flash, Split Gate, p-channel EEPROM, and Phase Change Memories. He was research scientist at STMicroelectronics in 2002, at Intel in 2003 and at Infineon Technologies in 2008. He participated in the research activity of several National and European projects.

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Erh-Nan Chou received the B.S. (1977) in Material Engineering from National Tsinghua University in Taiwan and the M.S. (1984) in Material Science and Engineering from North Carolina State University in Raleigh. Since then, he has been working for MMI, AMD, Philips and CSM Corp. in plasma etch process development field. Erh-Nan joined UMC since 1994 and worked for 14 years, majority in Quality management area as Q&RA Director until retiring at end of 2008. He holds one US patent in plasma etch.

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Chris Connor is the D1D Ramp Quality and Reliability manager in Hillsboro, Oregon. He has been at Intel Oregon for over eleven years working in front end integration and quality and reliability on the 180nm, 130nm, 65nm, 45nm, and 32nm process technologies. He has received one Intel Achievement Award for P4 Transistor enhancement, and is a member of the IEEE. Chris received his BSME from the University of Colorado at Boulder and his MSEE at The University of Texas at Austin.

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Dr. Edward Coyne graduated from the National University of Ireland, Galway in 1999 with a degree in Applied Physics and Electronics. From there he joined Analog Devices as a Product Analysis Engineer and completed a part-time Ph.D. on ultra-short pulsed laser interaction with silicon. In 2004, he transferred to the Development Department at Analog Devices, working on Technical Computer Aided Design (TCAD) and the integration of sensors for product development. In 2007 he joined NXP – Philips Semiconductors to pursue an interest in Transmission Electron Microscopy and analytical techniques.

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Olivier Crépel was born in France, in 1977. He received the B.S. and M.S. degrees, both in electrical engineering, from the Lille University of Sciences & technologies, in 2000 and 2001, respectively. From 2001 to 2004, he worked in the product analysis group of Philips Semiconductor, Caen, France, where he conducted research on magnetic microscopy techniques for failure analysis on ICs. He received the Ph.D.degree in 2004 in electrical engineering from the Caen University, France. In July 2004, he joined Freescale Semiconductor, Toulouse, France, in the Quality group, Product Analysis lab. He is currently the Electrical Engineering Manager.

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John D. Cressler received his Ph.D. in applied physics from Columbia University in 1990. He was on the research staff at IBM Research (1984-1992), the faculty of Auburn University (1992 to 2002), and currently is Ken Byers Professor of Electrical and Computer Engineering at Georgia Tech. His research interests center on silicon-based heterostructure devices and circuits, and he and his team have published over 450 papers in this area. He is the co-author of Silicon-Germanium Heterojunction Bipolar Transistors (2003) and the editor of Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits, and Applications of SiGe and Si Strained-Layer Epitaxy (2006). He has received a number of awards for both his teaching and research, and was elected Fellow of the IEEE in 2001.

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Kristof Croes received his BSc in physics at the Catholic University of Louvain (Belgium) in 1993 and his MSc in biostatistics at the Limburgs Universitair Centrum (LUC) in 1994. In 1999, he obtained his PhD, concerning the development of statistical techniques for planning reliability experiments. After that, he joined the reliability business unit of XPEQT, first as the software responsible and than as the manager of the R&D. From 2003 till end 2006, he was product and application manager of the package level reliability products of Chiron holdings. Beginning 2007, he went back to research, working as a BEOL reliability engineer in IMEC.

D'Andrade, Brian (2D.5)
In 1998, Dr. Brian D'Andrade began research on organic electronics under Prof. Tom Jackson at The Pennsylvania State University and then continued, until 2004, research on organic light emitting devices (OLEDs) with his advisor Prof. Stephen Forrest at Princeton University. He continued to research and develop white OLEDs with high efficacy and perdurable blue phosphorescent OLEDs while at Universal Display Corporation. His work led to white organic light source with over 100 lm/W efficacy and blue device with over 10,000 hrs of operational lifetimes.

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Francesca Danesin was born in Padova, Italy in 1980. She graduated in Electronics Engineering at the University of Padova in 2005. In January 2006 started the Ph.D. in Electronics and Telecommunications Engineering at the University of Padova. Her main research interests are in the field of reliability and characterization of GaN HEMTs devices.

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of journals and books, organized international conferences and symposia, and published over 200 articles in the scientific literature. He has won numerous awards including U.S. Department of Energy Outstanding Scientific Accomplishment Award (1989), Alexander von Humboldt Research Award (2002), ASM International Silver Medal (2003) and an IBM Faculty Award (2006).

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F. de Bruijn received his B.sc. degree in electrical engineering and computer science from the Hogeschool 's-Hertogensbosch, The Netherlands in June 1988. He worked 10 years for Digital Equipment Corporation mainly in quality and reliability engineering positions. In 2000 he joined Philips Semiconductors (now NXP) working on the release of products and processes. From 2004 onwards he worked on the quality and reliability aspects of BAW technology and packaging. Recently, he joined the base station group at NXP to release products and advanced LDMOS transistor technology.

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David De Roest was born in Bruges (Belgium) on September 24, 1975. He received his MS degree at the Department of Physical Engineering at the University of Ghent in 1998 and his Ph.D. entitled "Electrical characterization of low-k dielectrics and Cu interconnects" in 2003 at the University of Leuven, in collaboration with IMEC (Interuniversity MicroElectronics Centre). He is currently working at ASM International as a senior process engineer, with main focus at the processing and integration of Aurora® low-k dielectrics.

Degraeve, Robin (2A.5, 4A.5, 5C.2, PI.2, XT.13, XT.16)
Robin Degraeve received the M.Sc. degree in electrical engineering from the University of Gent, Belgium, in 1992, and the Ph.D. degree from the Catholic University of Leuven, Belgium, in 1998. He joined the Interuniversity Microelectronics Center (IMEC), Leuven, in 1992 in the CMOS Reliability group, where he is currently working as a Senior Researcher. His work has been focusing on reliability aspects of thin insulating layers under electrical stress. His current interests and activities include hot-carrier related reliability issues in MOSFETs, the study of the physics of degradation and breakdown phenomena in gate oxide films, the reliability of flash memory devices, the reliability of ultrathin oxide and oxynitride layers for VLSI technologies, and the reliability of high-k materials as MOSFET gate insulators for future CMOS generations.

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Jean-Michel Desmarres got his PhD in Materials Science from Limoges University in 1989 in the ceramics field. He started as Quality Material engineer at CNES and did technical support to CNES projects as expert materials. Since 2003, he is in Laboratories and Expertise Section of CNES where he is responsible of the materials and mechanisms activities. He is author or coauthor of more than 15 papers.

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Bart Desoete was born in Torhout, Belgium, in 1974. He received the M.S. degree in Engineering, option Physics, and the Ph.D. degree in Applied Sciences, from the University of Gent, Belgium, in 1997 and 2002, respectively. From 1997 to 2002, he was a researcher at the department of Electronics and Information Systems of the University of Gent, where he was involved in low power micro-electronics and solar energy thermodynamics. In 2002 he joined AMIS Belgium (currently On Semiconductor), where he started as a device modeling engineer in the technology department. In 2006 he moved to the device development group, where he is currently project leader and responsible for the industrialization of the XtreMOS technology.

Deyine, Amjad (3B.2)
Amjad Deyine obtained her Master Degree in Applied Physics from the National Institut of Applied Sciences of Toulouse (2006) and an equivalence from Polytechnique of Montreal (Canada). She is currently doing a Ph.D. on the development of Dynamic Laser Stimulation techniques for IC failure analysis. Since 2007 she works in the expertise laboratory shared between THALES and CNES (the French Space Agency) .

Dhennin, Jeremie (ME.1)
Jeremie Dhennin was born in 1983 in the North of France. After his engineering degree successfully obtained in 2005 he joined Nova MEMS' team as an R&D engineer. His microphysist profile permits him to focus his research activity on the study of the electro-mechanical properties of the materials used in MEMS, and on their influence on reliability.

Dion, Michael (2H.1, SE.4)
Michael J. Dion received the B.S. in electrical engineering with high honors from the University of Florida (1980) and joined Harris Semiconductor, Melbourne, Fl., as a reliability engineer. During his time at Harris he held various reliability engineering and supervisory positions and received the M.S. in electrical engineering (1988) from the University of Florida. Starting in 1987 he was involved in wafer-level reliability methodology development and was active with the JEDEC 14.2 Committee on Wafer-Level Reliability. In 1990 he was assigned by Harris to SEMATECH as a reliability physicist and later accepted the role as JEDEC 14.2 Chair in 1992. Upon return to Harris in 1993 he focused on process reliability and process control assurance, with later specialization in metal process reliability characterization. In 1999 he joined Intersil Corp. with continued focus on metal process reliability characterization and leadership of JEDEC 14.2. In 2005 he joined Rockwell Collins and is currently a commercial avionics Reliability, Maintainability and Safety Engineer, with focus on the avionics Safety impacts and characterization of Single Event Effects (SEE) on complex integrated circuits, including active participation in AVSI, mitigating radiation effects on current and future avionics systems.

Diop, Malick (2C.3)
Malick Diop received his M.S. degree in Physics from Blaise Pascal University of Clermont-Ferrand (France) in 2005 and his M.S. degree in Microelectronics and Microsystems from University of Rennes (France) in 2006. He is currently working with STMicroelectronics toward the PhD degree. His research focuses on reliability physics and low frequency noise on high speed SiGe: C HBT devices.

Djezzar, Boualem (EX.1)
Boualem Djezzar received his DEA (Master) degree in microelectronics from University1 of Grenoble, France and Master in thin film field from University of Algiers. He is in charge of research at Microelectronics and Nonotechnology Division of CDTA, Algiers, Algeria. He works on MOS devices reliability and electrical characterization of radiation-induced traps in silicon dioxide, SiO2 and interface, Si/SiO2 in MOS devices. He worked on process simulation and modeling of CMOS, BiCMOS, and CBiCMOS. In 1992, He was with LEPES Laboratory of CNRS, Grenoble, France where he worked on thin film deposition under ultra-high vacuum of Erbium Silicide on Si (111).

Dominik, Laura (SE.4)
Laura Dominik (Principle Systems Engineer and PMP at Honeywell) is the Chairperson for AVSI Task Group on Radiation Effects. Experience in the hardware, software and systems development of avionics and weapon systems, medical devices, and multi-service communications networks. Published in trade journals and authored industry standards across several industries including the most recent IEEE paper on "System Mitigation Techniques for Single Event Effects."

Donoval, Daniel (2D.6)
Daniel Donoval (Prof.) was born in Banská Bystrica, Slovakia in 1953. He received his MSc and PhD degrees in electronics from Slovak University of Technology in 1976 and 1981, respectively. Since 1981 he has been with Microelectronics Department, FEI STU Bratislava, where he is a Professor and Head of Department since 1994. His research interests include technology and characterization of semiconductor structures and devices supported by 2/3-D modeling and simulation. He is a member of Scientific Community Council and Education and Training Coordination Board of European Technology Platform ENIAC.

Doyen, Lise (IC.14)
Lise Doyen received the Engineering degree in materials and microelectronics from the Institut National des Sciences Appliquées, Toulouse, France, in 2005, and the Ph.D. degree in micro- and nanoelectronics from the Université Joseph Fourier, Grenoble, in 2009. Her dissertation focused on electromigration in advanced copper interconnects. in collaboration with the CEA-Leti/Minatec and the Science et Ingeniére des Matériaux et Procédés Laboratory, Grenoble, France. She is now with Central CAD Design Solutions, STMicroelectronics, Crolles, France, working on silicon integrity.

Du, G.A. (XT.10)
G. A. Du received the B.Eng. (Hons.) degree from the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, where he is currently working toward the Ph.D. degree under a Chartered-NTU Graduate Research Scholarship. His research project is on the characterization of bias-temperature instability in advanced P-MOSFETs. He is also developing novel ultrafast characterization techniques.

Du, Pei-Ying (3C.4, MY.1, MY.2)
Pei-Ying Du was born in Taipei, Taiwan in 1982. She received her B.S in engineering and system science from National Tsing-Hua University (NTHU) in 2004. She is currently pursuing the Ph.D. degree from the institute of electronics, National Chiao-Tung University (NCTU). She joined Emerging Central Lab. (ECL) in Macronix International (MXIC) in 2006, where her current research is engaged in reliability studies of nitride trapping Flash Memories.

Eklund, Bob (2C.4)
Bob Eklund (M ’85 – SM ’03- F ’03) received the B.S. degree in chemistry from Davidson College in 1974 and the Ph.D. degree in chemistry from the University of Texas at Austin in 1979. He joined Texas instruments Inc. in 1979 and has worked on numerous bipolar, BiCMOS, and sub-micron CMOS technology development programs. Currently, he is responsible for the technology roadmaps and development of high performance analog and BiCMOS technologies.

Ellis, David (5F.3, EL.5)
David Ellis is an Electrical Engineering Graduate Student at the University of Central Florida. With a Bachelor's in Computer Engineering, he approaches electrical engineering problems with the view of accelerating their solution time through automation. Gate Dielectric Breakdown is particularly interesting due to the unsolved problems in the fields of Physics, Chemistry, Reliability, and Electrical Engineering, with the semiconductor industry looking for breakdown simulation.

Endrinal, Lesly Zaren (3E.6)
Lesly Endrinal graduated from the University of the Philippines in 1999 with a Bachelors Degree in Electronics and Communications Engineering. She further continued her study to Master’s Degree level at the De La Salle University and at the same time, she is also working at Analog Devices. She joined Analog Devices Philippines in 2000 and worked as a Failure Analysis and Reliability Engineer. In 2005, she transferred to Intel Philippines, where she worked as a Product and Test Engineer. From 2006 till present, she is working as a Failure Analysis Engineer at NXP Semiconductors.

Enichlmair, Hubert (4C.4)
Dr. Hubert Enichlmair received his Master degree (1990) from university of Graz and the Ph.D. (1995) from the technical university in Linz, Austria. He joined austriamicrosystems in 1995 and has been engaged in device engineering with special interest in the reliability aspects of high voltage devices.

Esler, James (2D.5)
James R. Esler received the B.S. degree from Virginia Polytechnic Institute, Blacksburg, in 1981. He worked in the solar energy industry at Advanced Photovoltaic Systems and Energy Photovoltaics (EPV). He has worked at Universal Display Corporation (UDC), Ewing, NJ, since 2002

Esqueda, Ivan (2G.4)
Ivan S. Esqueda is currently working toward the Ph.D. degree in electrical engineering at Arizona State University, Tempe. His research interests include the analysis and modeling of radiation effects of advanced SOI and multiple-gate MOSFETs.

Euzent, Bruce (3A.2)
Bruce Euzent received a B.S. degree in EE from Cornell and M.S. from Carnegie-Mellon University. In 1974, he joined Intel Corporation working in engineering and later held various management positions. In 1991, he joined Weitek Corporation as Director of Q&R. Since 1995 he has been Vice President of Q&R at Altera Corporation. He is a member of IEEE and a past General Chairman of the IRPS. He has published several papers on reliability. Mr. Euzent is the chairman of The JEDEC committee on Silicon Devices Reliability, Qualification, and Monitoring. He is a member of the Advisory Board of MEPTEC.

Fang, Yi-Pin (SE.1)
Yi-Pin Fang recieved the M.S. (2000) and Ph.D. (2005) in Physics from National Tsing Hua Univ., Hsinchu, Taiwan. In 2005, he joined R&D Division of TSMC (Taiwan Semiconductor Manufacturing Co.) as a principal engineer. His research interests include soft-error-rate model setup and soft-error-rate reliability issues of memory and logic cells.

Fantini, Fausto (CD.4)
Fausto Fantini received the Laurea degree in electronic engineering from the University of Bologna. From 1973 to 1987, he was with Telettra, Vimercate, Italy. In 1987, he joined the SSSUP S.Anna, Pisa, as an Associate Professor. In 1990 he became Professor of Microelectronics at the University of Parma. Since 1997, he has been with the University of Modena and Reggio Emilia. His research interests are focused on device physics and reliability. He is currently one of the Editors of IEEE TDMR, member of the Editorial Board of Microelectronics Reliability and of the Steering Committee of ESREF.

Faqir, Mustapha (CD.4)
Mustapha Faqir was born in Morocco in 1979. He received the MS degree in Electronics Engineering from the University of Modena and Reggio Emilia, Italy. He worked for 2 years as a R&D engineer at MD Microdetectors, Modena, Italy. In 2009 he received the PhD in Electronics and Telecommunications from the University of Modena and Reggio Emilia, within the framework of an international doctorate agreement with the University of Bordeaux 1, France. He is currently holding a post-doc position at the University of Bristol, UK.

Fareed, Qhalid (2D.1)
Qhalid Fareed received his Ph.D. degree in Semiconductor Physics from Anna University, Chennai, India, in 1997. He has done extensive research at Prof. Sakai’s group in University of Tokushima,

Japan, on epitaxial and quasi-bulk growth of GaN. He has also worked at Sensor Electronic Technology Inc. Columbia, SC on III-nitride materials. He has published over 70 journal publications and presented about 50 papers in National/International conferences. He also worked as a Research Professor at the Photonics and Microelectronics lab of the University of South Carolina. His current research interests are deep UV LEDs, UV laser diodes, non-polar III-nitride laser diode and AlInGaN HEMT devices.

Feldmann, Klaus (3F.1)
Prof. Dr.-Ing. Klaus Feldmann, born in 1943, studied production engineering at the Technical University of Berlin. He earned his doctorate at the Institute of Professor Spur on his scientific research on design optimisation of automated lathes. After some years of working as a R&D manager in the fields of automation and assembly technology in Erlangen and as a production manager at a plant in Amberg he has become Head of the Institute for Manufacturing Automation and Production Systems (FAPS) at the University of Erlangen in 1982. He is speaker of some collaborative research areas, and chairman of the research association "Molded Interconnect Devices – 3D-MID". More over he is an active member of national and international science communities.

Ferguson, Phillip (SE.4)
Phillip D. Ferguson received a B.S. (1988), M. S. (1993), and Ph.D. (1995) in nuclear engineering from the University of Missouri-Rolla. He worked at Los Alamos National Laboratory as a graduate student in 1989, working on the Proton Storage Ring and designing experiments for the Los Alamos Spallation Radiation Effects Facility. In 1995 he joined the Manuel Lujan Neutron Scattering Center, working on the Accelerator Production of Tritium project and the Lujan Center Reliability Project, where he served as the target system neutronics lead. Phil moved to the Spallation Neutron Source at Oak Ridge National Laboratory in 2000. There he has served as the target system neutronics lead, the Neutronics Team Leader, and is currently the Neutron Source Development Group Leader.

Feustel, Frank (IC.6)
Frank Feustel is a member of technical staff in the process integration group of AMD's Fab36. He is involved in BEOL unit process development with a particular focus on reliability. He holds a Ph.D. in electrical engineering from the Dresden University of Technology.

Fichtner, Wolfgang (5F.1)
Wolfgang Fichtner (M'79–SM'84–F'90), a physicist, graduated at the Technical University of Vienna, Austria, in 1978. From 1979 through 1985, he worked at AT&T Bell Laboratories, Murray Hill, NJ. Since 1985 he is full Professor at ETH Zurich, Switzerland. In 1993, he founded ISE AG, a company in the field of Technology CAD (now the TCAD Business Unit of Synopsys, Inc.). He is a Fellow of the IEEE and a member of the Swiss National Academy of Engineering. In 2000, he received the IEEE Andrew S. Grove Award for his contributions to Technology CAD. His research activities cover physics based simulation of semiconductor devices and technologies in nanoelectronics, physical characterization and electronic measurement in nano-technologies as well as design and test of digital integrated circuits. Wolfgang Fichtner is author of 4 books and (co-)author of more than 500 reviewed scientific papers.

Filippi, Ronald (5A.2)
Ronald Filippi received his B.A. in Physics from Bucknell University in 1988, his M.S. in Materials Science from Polytechnic University in 1996 and his M.E. in Electrical Engineering from Rensselaer Polytechnic Institute in 2003. Since joining IBM in 1989, he has worked in reliability engineering at East Fishkill, New York, focusing on metallization and device failure mechanisms. Some of his technical areas of interest include electromigration, stress migration, thermal cycle and hot carrier degradation. He has authored or co-authored more than 40 articles in the areas of interconnect reliability and process development, and 21 patents related to semiconductor technology.

Frost, Christopher (SE.6)
Christopher Frost has been a scientist at ISIS, the UK's neutron source sited at the Rutherford Appleton Laboratory, since January 1998. He took his BA degree at Cambridge University where he stayed to complete a PhD in the Cavendish Laboratory in neutron science. At ISIS he has been immersed in scientific and technical development in both large and small projects and currently leads the development of electronic neutron irradiation facilities as part of the second target station at ISIS and the use of spin-polarised gases for neutron science in collaboration with the UK medical imaging and European neutron communities.

Fujieda, Shinji (2E.3, 4B.3)
Shinji Fujieda received the B.S. (1982) and M.S. (1984) in applied physics from Univ. of Tokyo, and the degree of Dr. Eng. from Tokyo Metropolitan Univ. (2004). After joining NEC Corp., Japan, in 1984, he worked on the process technology of compound semiconductor devices and is recently working on the reliability of CMOS gate stacks and non-volatile memories in Device Platforms Res. Labs. of NEC Corp. He is currently with Nano Electronics Res. Labs. of NEC Corp.

Fujii, Shosuke (4A.4)
Shosuke Fujii received the B.S. (2005) and M.S. (2007) in materials science and engineering from Kyoto University, Kyoto, Japan. he joined the Advanced LSI Technology Lab, Toshiba Corp., Yokohama, Japan, in 2007, where he has been engaged in the research on reliability physics of MISFET in high-k gate dielectrics.

Fujisawa, Takafumi (XT.9)
Takafumi Fujisawa was born in Nagano, Japan, on March 22, 1985. He received the B.S. degree in electronic engineering from Tohoku University, Sendai, Japan in 2008. He is currently working toward the M.S. degree in the Graduate School of Engineering, Tohoku University (MC1). His research interests are the development of processes suppressing the variability of MOSFETs and Random Telegraph Signal (RTS) noise.

Fukatsu, Shigeto (4A.2, 4A.4)
Shigeto Fukatsu, received the B.E. (2000), M.S. (2002), and Ph.D. (2005) in applied physics from Keio University, Japan. In 2005, he joined Advanced LSI Technology Laboratory, Toshiba Corporation, Yokohama, Japan. He has been engaged in the research on the reliability physics of MOSFETs.

Futase, Takuya (3E.1)
Takuya Futase received the B.S. and the M.S. degrees in material science and engineering from Muroran Institute of Technology, Hokkaido, Japan, in 1994 and 1996, respectively. He joined Hitachi ULSI Systems Co., Ltd., Tokyo, Japan, in 1996, and then he joined Trecenti Technologies, Inc. and Hitachi Ltd., Ibaraki, Japan, in 2001 and 2002, respectively. Since 2003 he has been working for Renesas technology Corporation, Ibaraki, Japan, where he is currently engaged in both of nickel silicidation and contact plug metallization of 300-mm single-wafer manufacturing for advanced logic devices. Mr. Futase is a member of Japan Society of Applied Physics.

Gadlage, Matthew (2G.3)
Matthew J. Gadlage received his B.S. in electrical engineering from the University of Evansville in 2002, and his M.S. in electrical engineering from Vanderbilt University in 2004. Since 2002, he has been a member of the Radiation Sciences Branch at Crane Naval Surface Warfare Center. He is currently working on his Ph.D. in electrical engineering at Vanderbilt University.

Gambino, Jeff (5B.1)
Jeff Gambino received the B.S. degree in materials science from Cornell University in 1979, and the Ph.D. degree in materials science from the Massachusetts Institute of Technology in 1984. He joined IBM, Hopewell Junction, NY, in 1984, where he worked on silicide processes for Bipolar and CMOS devices. In 1992, he joined the DRAM development alliance at IBM's Advanced Semiconductor Technology Center. While there, he developed contact and interconnect processes for three generations of DRAM products. In 1999, he joined IBM's manufacturing organization in Essex Junction, VT, where he has worked on copper interconnect processes for CMOS logic and CMOS imager technology. He has published over 100 technical papers and holds over 100 patents.

Garrett, Gregory (2D.2)
Gregory A. Garrett received the B.S. degree in engineering physics from Cornell University, Ithaca, NY, in 1992, and the Ph.D. in applied physics from the University of Michigan at Ann Arbor, in 2001. He is currently a Research Physicist at the U.S. Army Research Laboratory, Adelphi, MD, in the Sensors and Electron Devices Directorate. The focus of his research is on carrier dynamics, studied by time-resolved optical spectroscopy techniques, in III-Nitride materials for optoelectronics.

Garros, Xavier (4A.3)
Xavier Garros received the M.S. in physics engineering, from the National Polytechnics Institute of Grenoble, France (2000) and his Ph.D. from the Univ. of Marseille, France (2004), on the physics and electrical properties of High-K dielectrics as the replacement of SiO2 for the future CMOS technologies. He joined the CEA-LETI in 2004 to work on the reliability of the High-K dielectrics. He has a deep knowledge in electrical characterization, physics and modeling of the reliability concerns related to High-K/Metal gate integration (N&PBTI, mobility, Ig, Vt…). During these last years, he has presented his work as first or second author at the IEDM, IRPS and VLSI conferences.

Gattel, Francesco (2B.1)
Francesco Gattel received the Laurea Degree in Computer Science Engineering from University of Modena - Italy, in 2000. He joined STMicroelectronics- Agrate (MI) in 2001, working in the Compact Modeling Team until 2008. His activities covered electron device compact modeling, with focus on automotive technology platforms, model card extraction flows and modeling of MOSFET aging effects. At the end of 2008 he moved to NAND flash memory design team, Numonyx-Agrate (MI).

Geinzer, Thomas (FA.1)
Thomas Geinzer studied electrical engineering at the University of Cooperative Education Ravensburg, Germany, gaining his Bachelor in 2003. He continued his studies at the University of Wuppertal and received his Master degree within the Faculty of Electrical, Information and Media Engineering. Now he is PhD student at the Department of Electronics of the University of Wuppertal.

Ghidotti, Michele (3C.1)
Michele Ghidotti was born in Cremona, Italy, in 1981. He received the Bachelor and Master degree in Electrical Engineering from Politecnico di Milano, Milano, Italy, in 2003 and 2006, respectively. He is currently with the Dipartimento di Elettronica e Informazione (DEI) of the Politecnico di Milano, where he is pursuing the Ph.D. working on experimental characterization and modeling of ultra-scaled Flash memory reliability.

Giai Gischia, Gianni (IC.9)
Gianni Giai Gischia is a Ph.D student at the Catholic University of Leuven, Belgium.

Gill, Balkaran (2H.3)
Balkaran Gill received the B.E. degree in electronics and communication engineering from Gulberga University, Gulberga, India in 1998 and the M.S. and Ph.D. degrees in computer engineering from the Case Western Reserve University, Cleveland Ohio in 2002 and 2005 respectively. Dr. Gill worked with IROC Technologies in 2003 and 2004. He is currently a component design engineer in architecture for quality and reliability with Intel Corporation, Hillsboro, Oregon. His interests are modeling and mitigation of transient errors and robust circuit design methodologies for low power systems. He has published more than ten technical papers and holds several pending U.S. patent

Glowacki, Arkadiusz (2C.2)
Arkadiusz Glowacki received the M.S. degree in electrical engineering from the Technical University of Lódź, Łódź, Poland, in 2003, focusing on the simulations of thermal transport and cooling efficiency in advanced cooling components. He is currently working toward the Ph.D. degree at the Berlin University of Technology, Berlin, Germany. His research interests include thermal and photonic laser stimulation techniques, as well as photon emission microscopy of semiconductor devices.

Gopalakrishnan, Vasudevan (3B.1)
Vasudevan Gopalakrishnan is currently Director of Test Engineering at T-RAM Semiconductor, and has over 20 years experience in the field of semiconductor test. He works closely with the Design, Technology and Reliability teams to define and execute a broad range of testing. He has been an author on numerous technical papers regarding T-RAM technology. Prior to joining T-RAM Semiconductor, he worked at Texas Instruments (INDIA), Advantest (SINGAPORE) and Alliance Semiconductor (SANTA CLARA,CA). At Alliance Semiconductor, he managed multiple product lines, including DRAM, SRAM, FLASH and Networking. He received a Bachelors degree in Electronics from Coimbatore Institute of Technology,INDIA.

Gornik, Erich (4C.6)
Erich Gornik has studied at the Technical University of Vienna, where he finished his Ph.D. in 1972.
He was Postdoc from 1975 to 1977 with the Bell Laboratories. From 1979 until 1988 he was full Prof. for Experimental Physics at the University of Innsbruck from where he changed to the Technical University of Munich as director of the Walter Schottky Institute. Since 1993 he is full Prof. for Semiconductor Electronics and since 1995 he is head of the Microstructure Center at the Technical University of Vienna. His main expertise is current transport and mid-infrared to far-infrared emission spectroscopy of semiconductor nanostructures.

Gos, Wolfgang (5D.2, XT.17)
Wolfgang Gös was born in Vienna, Austria, in 1979. He studied Technical Physics at the Technische Universiät Wien, where he received the degree of Diplomingenieur in 2005. His diploma thesis addressed grain boundaries in back contact solar cells. He joined the Institute for Microelectronics in January 2006, where he is currently working on his doctoral degree. In 2007, he was a visitor at the Vanderbilt University, Deptartment of Physics and Astronomy, in Nashville, TN. His current scientific interests include first-principles simulations of the chemical processes involved in NBTI and HCI, modeling of tunneling and charge trapping, reliability issues in general.

Gossner, Harald (6C.3, EL.2)
Harald Gossner received the degree in physics (Dipl.Phys.) from the Ludwig–Maximilians University, Munich, Germany, in 1990, and the Ph.D. degree in electrical engineering from the Universität der Bundeswehr, Munich, in 1995. Since 1995, he has been with Infineon technologies AG, Munich, working on the development of ESD

protection concepts for bipolar, BiCMOS, and CMOS technologies. He is the Head of the team of Infineon's center of competence for ESD and external latchup development and also a Senior Principal who guides the company activities in the field of overvoltage robust design. He has authored and coauthored more than 40 technical papers and one book in the field of ESD. Dr. Gossner is a member of the management board of the International ESD Workshop (IEW) and a Cochair of the Industry Council on ESD Target Values. He is serving in the TPC of EOS/ESD Symposium, IEDM, and IEW.

Goto, Masakazu (4A.2, 4A.4)
Masakazu Goto received the B. E. and M. E. degrees in applied physics from University of Tsukuba, Tsukuba, Japan, in 2003 and 2005, respectively. He joined the Center for Semiconductor Research & Development of Toshiba Semiconductor Company, Yokohama, Japan, in 2005. His current work is the development of metal gate / high-k CMOS devices. He is a member of the Japan Society of Applied Physics.

Grasser, Tibor (2A.1, 2A.2, 2B.2, 2B.5, 5D.2, XT.17)
Tibor Grasser received his Ph.D. degree in technical sciences from the TU Wien where he is currently employed as an Associate Professor. In 2003 he was appointed head of the Christian Doppler Laboratory for TCAD in Microelectronics. Dr. Grasser is the co-author or author of over 250 scientific articles, editor of a book on advanced device simulation, a senior member of IEEE, has been involved in the program committees of SISPAD, IWCE, ESSDERC, IRPS, IIRW, and ISDRS, and is a recipient of the Best Paper Awards at IRPS and ESREF. He was also a chairman of SISPAD 2007.

Groeseneken, Guido (2A.5, 2B.5, 4A.5, 5C.2, PI.2, XT.13, XT.16)
Dr. Guido Groeseneken received the M.Sc. degree in electrical and mechanical engineering (1980) and the Ph.D degree in applied sciences (1986), both from the Katholieke Universiteit Leuven, Belgium. In 1987 he joined the R&D Laboratory of IMEC (Interuniversity Microelectronics Center) in Leuven, Belgium, where he is responsible for research in reliability physics for deep submicron CMOS technologies. From October 2005 until April 2007 he was also responsible for the IMEC Post CMOS Nanotechnology program within IMEC's core partner research program. Since 2001 he is also Professor at the KU Leuven,where he is Program Director of the Master in Nanoscience and Nanotechnology, and where he is also coordinating a European Erasmus Mundus Master program in Nanoscience and nanotechnology. He became an IEEE Fellow in 2005 and an IMEC Fellow in 2007. He has made contributions to the fields of non-volatile semiconductor memory devices and technology, reliability physics of VLSI-technology, hot carrier effects in MOSFET's, time-dependent dielectric breakdown of oxides, Negative-Bias-Temperature Instability effects, ESD-protection and – testing, plasma processing induced damage, electrical characterization of semiconductors and characterization and reliability of high k dielectrics. Recently he has also interest in nanotechnology for post-CMOS applications, such as carbon nanotubes for interconnect applications, tunnel FET's for alternative nanowire devices etc. He has served as a technical program committee member of several international scientific conferences, among which the IEEE International Electron Device Meeting (IEDM), the European Solid State Device Research Conference (ESSDERC), the International Reliability Physics Symposium (IRPS), the IEEE Semiconductor Interface Specialists Conference (SISC) and the EOS/ESD Symposium. From 2000 until 2002 he also acted as European Arrangements Chair of IEDM. In 2005 he was the General Chair of the Insulating Films on Semiconductor (INFOS) conference, organized in Leuven, Belgium. He has authored or co-authored more than 500 publications in international scientific journals and in international conference proceedings, 6 book chapters and 10 patents in his fields of expertise.

Gu, Shaw-Hung (MY.4)
Shaw-Hung Gu was born in Taipei, Taiwan, R.O.C. on August 11, 1977. He received the B.S. degree from Chang-Gung University, Taoyuan, Taiwan, R.O.C., in 1999, and the M.S. and Ph.D. degree in electronics engineering from the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2001 and in 2006. Then, he joined Macronix International Company, Ltd. and is responsible for the developement of nitride-based storage memory.

Gupta, Rajesh (3B.1)
Rajesh Gupta is currently Manager of Technology Development at T-RAM Semiconductor, where he has worked since 2001. His group develops manufacturable Thyristor-based memories. Prior to this, he developed a broad range of power devices at Rockwell Science Center. He holds 7 patents and has published over 15 technical papers. He received a M.S. degree in Electrical Engineering (1998) from Rensselaer Polytechnic Institute (RPI) and a B.S. degree (1996) from the Indian Institute of Technology(IIT) at Madras. He received the Henry J. Nolte award for best academic performance at RPI and the Ramasarma Kolluri medallion for best academic performance at IIT.

Gupta, Satrajit (XT.15)
Satrajit Gupta received his PhD in Electrical and Computer Engineering from Carnegie Mellon University, Pittsburgh, PA in 2004, MS in Microelectronics from the Indian Institute of Science, Bangalore, India in 1999 and BS in Electrical Engineering from the Birla Institute of Technology and Science, Pilani, India in 1997. He was a winner of the best student paper award in the International Conference on VLSI Design, Goa, India in 1999. His research interests are in the area of reliability, statistical modeling and modeling electron transport in nanostructures.

Gusmeroli, Riccardo (3C.1)
Riccardo Gusmeroli was born in Morbegno, Italy, in 1979. He received the Laurea degree in Electronics Engineering (2003) and the Ph.D. degree (cum laude) in Information Technology (2007) from the Dipartimento di Elettronica e Informazione, Politecnico di Milano, Milan, Italy. His research activity focuses on modeling and characterization of advanced MOS and memory devices, and on the development of circuits and systems for biological signal sensing and processing. Dr. Gusmeroli also cooperated with the Dipartimento di Fisica, Politecnico di Milano, Milan, Italy and the European Synchrotron Radiation Facility, Grenoble, France, on X-ray spectroscopy.

Hada, Hiromitsu (2E.3, 4B.3)
Hiromitsu Hada received the B.E. and M.E. degrees in electrical engineering from Mie University, in 1982 and 1984, respectively. In 1984, He joined NEC Corporation, Kawasaki, Japan, where he was involved with CMOS SOI LSIs, DRAM and FeRAM technology. He is currently involved in the research and development of non-volatile memory technology at the Device Platforms Research Laboratories, NEC Corporation, Kanagawa, Japan.

Hajjar, Jean-Jacques (5F.3, EL.5)
Jean-Jacques Hajjar received the B.S, M.S and PhD degrees from the Massachusetts Institute of Technology, Cambridge, MA, in 1983, 1985 and 1989 respectively. He is currently the manager of the Corporate ESD Department at Analog Devices, Wilmington, MA. Dr. Hajjar is focused on improving ESD and latchup robustness for all Analog Devices products. Prior to his current role, Dr. Hajjar was involved, also at Analog Devices, in fully-isolated bipolar IC process development and SPICE device modeling for predictive circuit Simulations.

Hamada, Kotaro (EL.4)
Kotaro Hamada was born in Osaka, Japan, on October 26, 1962. He received the B.S. and M.S. degrees in materials from Osaka

University, Osaka, in 1986 and 1988, respectively. In 1988, he joined the Analysis Technology Research Center, Sumitomo Electric Industries, Ltd., Osaka, Japan, where he has been engaged in research and development of analysis technology of materials. He is a member of the Japan Institute of Metals and the Japan Society for Analytical Chemistry.

Han, Tzung-Ting (MY.4)
Tzung-Ting Han was born in I-Lan, Taiwan, ROC., on November 18, 1973. He received the B.S. degree in engineering science from National Cheng Kung University, Tainan, Taiwan, R.O.C. in 1997 and the M.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, R.O.C. in 1999. In 1999, he joined Macronix International Co., Ltd., Hsinchu, Taiwan, to work on advanced diffusion module process development. Since 2002, he has worked on process integration of advanced non-volatile memory.

Hara, Naoki (2C.1)
Naoki Hara was born in Tokyo, Japan in 1963. He received the B. E., M. E., and Ph. D degrees from the University of Tokyo, Tokyo, Japan, in 1985, 1987, and 1990, respectively. In 1990, he joined Fujitsu Ltd., Kanagawa, Japan, where he engaged in the research and development of HEMTs and other heterostructure devices. Dr. Hara is a member of Institute of Electrical and Electronics Engineers, and the Institute of Electronics, Information and Communication Engineers, Japan, and the Institute of Electrical Engineers of Japan, and the Japan Society of Applied Physics.

Harmon, David (XT.12)
David Harmon received a B. S. degree in 1977 and an M. S. degree in 1979, both in electrical engineering from the University of Maine. Since joining IBM in 1979, he has worked in the areas of plasma process development, ASIC applications, and technology reliability engineering. David is currently a Senior Engineer in the IBM Semiconductor Solutions Divsion and is the author of more than 35 publications. His primary interests are the study of reliability mechanisms for integrated circuits and the development of science education units for K-12 classrooms.

Hartranft, Marc (FF.1)
Marc Hartranft received his BS in Electrical Engineering from Michigan Technological University in 1977. Marc joined Cisco, Inc in August of 2006 where he has led the team responsible for Component Engineering for all memory IC's and modular solutions in FLASH, DRAM, SRAM, TCAM, E2PROM and EPROM components. He has held various engineering and management positions at Honeywell Inc., Zilog and Cypress Semiconductor. Marc holds 13 patents relating to semiconductor process technology and circuit design, ESD protection in integrated circuits and opto-electronic components.

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Tsuyoshi Hasegawa received the B. S. degree in physics in 1985, the M. S. degree in materials science in 1987, and the Ph. D degree in Physics in 1996 from the Tokyo Institute of Technology. He has conducted the Atomic Electronics Group in the National Institute for Materials Science (NIMS) as the Group Leader since 2003. He is also the Principal Investigator of International Center for Materials Nanoarchitectonics (MANA) since 2007.

Hasunuma, Ryu (3E.5)
Ryu Hasunuma was working at Texas Instruments Japan Ltd., and engaged in developing atomic manipulation technique with a scanning tunneling microscope. He was also focusing on characterization of ultra-thin SiO2 films, and received his PhD in 2001. He started a carrier at University of Tsukuba in 2003, and has been focusing on reliability issues in gate dielectrics for future LSI devices with a combination of electrical analysis and nano-scale.

Hayes, Dennis (3B.1)
Dennis Hayes received the B.S. degree in Biology from San Diego State University. After graduating he spent ten years as a contractor to NASA, Ames Research Center, Mountain View, California in the field of atmospheric sciences. While at NASA he completed graduate course work in Environmental Management at the University of San Francisco. He then began an 18 year career at Hewlett-Packard/Agilent Technologies in various capacities including: materials characterization, parametric test, reliability, and packaging. He is currently engaged in parametric test at T-RAM Semiconductor.

Hehenberger, Philipp (2B.2, XT.17)
Philipp Hehenberger was born in Vienna, Austria, in 1980. He studied technical physics at the Technische Universität Wien, where he received the degree of Diplomingenieur in December 2006. He joined the Institute for Microelectronics in January 2007, where he is currently working on his doctoral degree. His current scientific interests include Fast-IdVg, OTF, OFIT and CP-Measurements, as well as device simulation and modeling of negative bias temperature instability and hot carrier effects.

Heiderhoff, Ralf (3E.4, FA.1)
Ralf Heiderhoff received his diploma in physics at the University of Wuppertal. 1997 he got his PhD in electrical engineering and became head of the group: "Optical and Thermal Microscopy Techniques". 1999 to 2000 he was Visiting Lecturer at the National University of Singapore followed 2001 by a Visiting Professorship at the Belarusian State University of Informatics and Radioelectronics and 2008 at the Beijing University of Technology. Since 2005 he has been in the management of the Institute of Polymer Technology. His major research is focused on measurements in the nanometer range and the combination of microscopes to hybrid systems.

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Tony F. Heinz is the David M. Rickey Professor in the Departments of Physics and Electrical Engineering at Columbia University. He received a BS degree in physics at Stanford University in 1978 and a PhD degree in physics at the University of California, Berkeley in 1982. He subsequently joined the IBM Watson Research Center in Yorktown Heights, where he stayed until joining Columbia University in 1995. His research activities focus on the electronic properties and dynamics of materials, particularly with respect to interfaces, thin-films, and nanostructured systems.

Heinzl, René (5D.2)
René Heinzl was born in Vienna, Austria, in 1977. He studied electrical engineering at the Technische Universität Wien, where he received the degree of Diplomingenieur in 2003 and his PhD in technical sciences in 2007. In April 2005 he achieved first place in the doctoral competition at the EEICT in Brno. His research interests include programming paradigms, high performance programming techniques, data structural aspects of scientific computing, performance analysis, process simulation, solid modeling, scientific visualization, algebraic topology, and mesh generation and adaptation for TCAD.

Herwik, Stanislav (E5.3)
Stanislav Herwik received the Diploma degree in microsystem technology from the Department of Microsystems Enigneering (IMTEK), University of Freiburg, Freiburg, Germany in 2006. In his thesis at Endress+Hauser, Maulburg, Germany he adressed the fluid density measurement with a vibrating fork. In April 2006 he joned the NeuroProbes team at the Laboratory for Microsystems Materials, Department of Microsystems Engineering (IMTEK), University of Freiburg and started his work on the development of silicon based neural probe arrays as a PhD student.

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Jeffrey Hicks is a Senior Principle Engineer in Intel's Technology Development Quality and Reliability Group and was the Q&R Program Manager for Intel's 45nm HK+MG technology. He received his B.S. degree in Applied Physics from Caltech in 1980 and joined Intel's Technology Development Group in Santa Clara CA in that year as a Reliability Engineer working on Bipolar and EPROM non-volatile memory technologies. In his years at Intel to date Mr. Hicks has served in numerous Quality and Reliability functions spanning Technology Development, manufacturing, Product, and Customer Quality and Reliability. He has several patents received or pending and has published a number of technical papers including Best Paper at the 1999 International Reliability Physics Symposium. He is the recipient of three Intel Achievement Awards.

Higgins, Robert (4C.5)
Robert Higgins received his B.S. in Engineering Physics (1991), and M.S. in Chemical Engineering (1995) from the Colorado School of Mines, and joined Texas Instruments in 1996. His focus has been on analog technology reliability development, including high-voltage and bipolar transistor hot carrier degradation, gate oxides, NBTI, and electromigration. He is a senior member of the technical staff at Texas Instruments, and a Certified Reliability Engineer (CRE). He is also an active member of the JEDEC 14.2 Wafer Level Reliability Standards Committee.

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Stefan Hillebrecht received his diploma in computer since 2005 from the Albert-Ludwigs-University of Freiburg. Today he is Ph.D. Student at the University of Freiburg. His research interests are testing of interconnect open faults and reliability of microelectrical mechanical systems (MEMS).

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Hirose, Yukinori (3E.1)
Yukinori Hirose received the B.S. (1985) and the M.S. (1987) degrees in faculty of engineering from Tohoku University, Sendai, Japan, and received the Ph.D. of engineering (2007) from Osaka City University, Osaka, Japan. Since 1987 he had been engaged in development of advanced process evaluation and failure analysis technology for the LSI Research & Development Laboratory, Mitsubishi Electric Corp. In 2003 he joined Renesas Technology Corporation. Also, he is a member of the Japanese Society of Microscopy, the Japan Society of Applied Physics, and the Japan Institute of Metals.

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Ho Heng Wah received his Bachelors of Electrical Engineering from the National University of Singapore in 2004. Since then, he has been working towards his PhD degree under a National University of Singapore Research Scholarship. His research interest is in the use of Scanning Thermal Microscopy for integrated circuit failure analysis.

Hoffmann, Thomas (4A.5, XT.13)
Thomas Hoffmann received a Ph.D. degree from Lille University, France, in 2000. He then joined Intel Corporation's R&D group in Hillsboro, Oregon, as a TCAD engineer for sub-90nm technologies. In 2004, he moved to Intel's technology development group as a device engineer for 45nm process development. In 2005, he joined IMEC in Leuven, Belgium, to lead the electrical characterization group for advanced silicon technologies. He has authored or co-authored approximately 50 technical papers for publication in journals and presentations at conferences.

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Ralf Hofmann is a Member of Technical Staff in the Advanced Technology Group under the Office of the CTO at Applied Materials. His work involves the evaluation and development of new processing techniques and equipment for new and emerging applications in the IC space as well as the energy sector. He joined Applied Materials in 1994 in the PVD Technology group, working on various aspects of metal deposition and process integration. In 2001 he joined ZMD America, Inc., a mixed-signal ASIC design company, where he worked on two successfully productized IC designs. He worked from 2002 to 2003 as an independent consultant for a telecommunications start-up company as well as a small company in the transportation sector before rejoining Applied Materials in 2004. Mr. Hofmann received a Diplom-Ingenieur degree in Electrical Engineering (MSEE) from Chemnitz University of Technology in Germany.

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Hsiao, Yi-Hsuan (3C.5)
Yi-Hsuan Hsiao was born in Chia-Yi, Taiwan in 1980. He received his B.S and M.S degrees in electrical engineering from National Chiao-Tung University (NCTU) in 2002 and 2004, respectively. His M.S thesis focused on TFT devices. He joined Emerging Central Lab. (ECL) in Macronix International. Co. (MXIC) in 2005, where his current research is engaged in developing new nonvolatile memory devices with TCAD simulation.

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Jung-Yu Hsieh was born in Hsinchu, Taiwan, R.O.C., in 1971. He received the B.S. degree in chemical engineering from the National Tsing Hua University, Hsinchu, Taiwan, in 1995, and the M.S. degree in chemical engineering from the National Tsing Hua Unive

Hsieh, Kuang-Yeu (3C.4, 3C.5, MY.1)
Kuang-Yeu Hsieh was born in Tainan Taiwan in 1958. He received his B.S (Physics) and MS (Materials Science) degrees from National Tsing-Hua University (NTHU) and National Sun Yet-sen University (NSYSU) in 1980 and 1985, respectively. He obtained his Ph.D. at North Carolina State University in Materials Science in 1989. Before he joined Macronix International in 2001, he had been an Associate Professor at Institute of Materials Science in National Sun Yet-sen University since 1992. His research interests includes MBE thin film growth, characterization of material, solid-state physics, IC fabrication, and optoelectronic materials. Currently, he is Director of Nano-technology R & Div./Emerging Central Lab in Macronix and involves in developing new nonvolatile memory devices and exploring new material for the next generation nonvolatile memory. Meanwhile, he has more than 70 journal papers published and 15 patents granted.

Hsu, Chih-Wei (MY.4)
Chih-Wei Hsu was born in Taipei, Taiwan, R.O.C., on August 17, 1981. He received the B.S. degree from Chang-Gung University, Taoyuan, Taiwan, in 2003 and the M.S. degree in electronics engineering from the National Chiao-Tung University, Hsinchu, Taiwan, in 2005. His research interest focuses on nitride storage Flash memory, especially in numerical simulation of the retention behavior.

Hsu, Tzu-Hsuan (3C.5, MY.1)
Tzu-Hsuan Hsu received the B.S. and M.S. degrees from the Department of Electrical Engineering and Institute of Microelectronic Engineering, National Cheng-Kung University, Tainan, Taiwan, R.O.C., in 2000 and 2002, respectively. He is currently pursuing the Ph.D. degree from the Institute of Electronics, National Tsing-Hua University, Taiwan, R.O.C. He joined Macronix International Company, Ltd., Hsinchu, Taiwan, R.O.C., in 2002 working on nanodevice research and development. His current research areas include high-density memory development, nitride-trapping memory devices, and advanced nonvolatile memory technologies.

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Huang, Rei-Fu (EL.3)
Rei-Fu Huang is a senior engineer at Media Tek in Hsinchu City, Taiwan. His research interests include VLSI testing, embedd-memory testing and repair, and MRAM testing. Huang has a BS and PhD in electrical engineering from National Tsing Hua University.

Huang, Bo-Shih (EL.3)
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Huang, Cheng (3A.2)
Dr. Cheng H. Huang received his BSEE from National Cheng Kung University in 1967, MSEE from National Chao Tung University in 1969, and PhD in device physics from University of Southern California in 1977. He worked for Intel Corporation in various reliability groups including technology reliability, manufacturing reliability, and product reliability from 1977 to 1995. He has been working for Altera Corporation in silicon reliability group since 1995. He has received 17 patents in noble devices.

Huang, D. (XT.1)
D. Huang received the B.S. degree in Physics from Fudan University, Shanghai, China, in July 1982 and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana, in December 1989.From December 1989 to May 1991, he was a Postdoctoral Research Associate with the University of South Florida, Tampa. Since June 1991, he has been a member of the faculty at Fudan University,as a Professor, in 1995, with the Physics Department,where he worked on the optical properties of semiconductor quantum wells, superlattices, and heterostructures and where,since 2005, he has been with the State Key Lab of ASIC and System, School of Microelectronics as a Professor. He was a visiting scientist with Virginia Commonwealth University, Richmond, from November 2000 to November 2002. His current research interest includes the reliability of Si microelectronic devices.

Huang, I-Jen (MY.4)
I-Jen Huang received the B.S. degree in electrical engineering from National Taiwan University, Taiwan, in 1992, and the M.S. degree in electrical engineering from National Taiwan University in 1994. He joined Macronix International Co., Ltd., Hsinchu, Taiwan, in 1996 as a process integration engineer. He has worked on process integration of non-volatile memory and SRAM for several generations. He is presently engaged in array characterization of NVM products.

Huang, Tiao-Yuan (3C.4)
Tiao-Yuan Huang received his Ph.D. degree from the University of New Mexico, Albuquerque, NM, in 1981. After working in the U.S. semiconductor industry for 14 years, he returned to his native country, Taiwan, and has since been a professor with National Chiao-Tung University (NCTU), Hsinchu. Prof. Huang was elected an IEEE Fellow in 1995 for his invention and demonstration of fully-overlapped lightly-doped-drain MOS transistors.

Huang, Tsui Hua (FA.2)
T. H. Huang, born in Ping-tung in 1963, is a staff engineer of UMC Corporation. Huang has been working in UMC over 24 years and has ever occupied a variety of positions across many divisions during this period of time. Now, she is a very experienced FA engineer and a good instructor in the Lab. Besides, she is a living dictionary about the history of this semicondutor IC manufacturer, UMC.

Huard, Vincent (5D.4, 6B.1)
Vincent Huard received the B.S. (1996) in physics and the M.S. (1997) in electrical engineering from the Institut National Polytechnique de Grenoble (INPG). He worked for the CEA-Grenoble on the MBE growth of II-VI based doped heterostructures and their magneto-optical and electrical characterizations. He received his Ph.D. (2000) in physics from the university of Grenoble. In 2000 and 2001, he was a Visiting Scholar at the University of California, where he worked on devices made of ferromagnetic materials on top of semiconductors. In 2002, he joined Philips Semiconductors as a reliability engineer, working on oxide and device reliability. Since 2007, he is at STMicroelectronics as Design-in Reliability project leader, working on device and circuit reliability modeling and product qualification tests. His current research

interests include NBTI and hot carrier degradation both at wafer and product levels as well as Design for reliability. He authored and co-authored more than 70 regular papers, several invited papers and is IRPS 2009 Circuit Reliability Chairman.

Hughes, Greg (BD.1)
Greg Hughes obtained a B.Sc in Chemistry from the University of Ulster in 1979 and subsequently received a PhD in studies of electronic states at metal semiconductor interfaces from the same University in 1983. Following two years post-doctoral research on the modification of semiconductor surface and interface properties in the IBM research division at Yorktown Heights, he joined the School of Physical Sciences at Dublin City University (DCU) on the lecturing staff. He spent the 1993/94 academic year on sabbatical at the Technical University of Berlin on an Alexander von Humboldt research fellowship. He was appointed as Visiting Research Associate Professor at Boston University in the summer of 2001. In May 2006, he was appointed Associate Professor in Physics in DCU and is a surface science research group leader in the National Centre for Sensor Research (NCSR). He has published over eighty papers in the field of surface science and has supervised 7 PhD and 4 MSc students through to completion. His current research team consists of 5 postgraduate students working on projects relating to the growth and characterisation of materials used in the semiconductor industry.

Hur, Chang-Hyun (MY.8)
Chang-Hyun Hur received the B. S. degree in Material Science from Hanyang University, Seoul, Korea,in 2000. He joined Samsung Electronics, Kiheung, Korea, where he has developed SRAM, UtRAM from 2000 to 2002. Since 2003 he has been engaged in 120 nm SLC and 90nm, 65 nm MLC NOR flash memory integration and yield enhancement activities.

Hurley, Paul (BD.1)
Paul Hurley received his Ph.D. (1990) and B.Eng.(1985 - First class honors) in Electronic Engineering at the University of Liverpool. He is a Senior Research Scientist at the Tyndall National Institute, University College Cork where his work focuses on high dielectric constant (high-k) materials intended for use as gate level insulators in transistors for future integrated circuits. The emphasis of his current research is the formation and characterisation of high-k films on silicon and III-V semiconductor substrates. Paul is a member of the Technical Committee of the Insulating Films on Semiconductors (INFOS) conference and the International Workshop on Dielectrics in Microelectronics (WoDiM). In addition to research activities, he is a part time lecturer in the Department of Microelectronic Engineering at University College Cork. He has published over sixty papers in the field of microelectronics.

Hwang, Cheol Seong (XT.3)
Cheol Seong Hwang received the M.Sc. and Ph.D. degrees from Seoul National University, Seoul, Korea, in 1989 and 1993, respectively. In 1994, he joined Samsung Electronics as a Senior Researcher. Since 1998, he has been a Professor at the Department of Material Science and Engineering, Seoul National University. He has authored or coauthored more than 240 papers in international peer-reviewed scientific journals, which are cited more than 3000 times, and has given 40 invited presentations in international conferences. His current interests include high-k gate oxide, DRAM capacitor, new memory devices including PRAM/RRAM, and ferroelectric materials and devices.

Hwang, Hyunsang (MY.5)
Hyunsang Hwang received the B.S. degree in metallurgical engineering from Seoul National University, Seoul, Korea, in 1988, and the Ph.D. degree in materials science from the University of Texas at Austin in 1992. From 1992 to 1997, he was with the LG Semicon Corporation, Cheongju, Korea, as a Principal Researcher. In 1997, he joined the faculty at Gwangju Institute of Science and Technology, Gwangju, Korea, as a Professor in the Department of Materials Science and Engineering. Recently, he has engaged in research on process, device design and reliability of high-k gate stack, and memory devices (ReRAM and Flash).

Hwang, Seongmo (2D.1)
Seongmo Hwang (S'06) received the B.S. degree in physics from University of Seoul and M.S. degree in physics from Seoul National University, Seoul, South Korea, in 2003 and 2005 respectively. He is currently a Graduate Research Assistant with the Photonics & Microelectronics Laboratory (PML), Electrical Engineering Department, University of South Carolina, Columbia since 2006. His research interests include study on III-Nitride based wide-bandgap semiconductor device physics such as light-emitting diodes (LEDs), laser diodes (LDs), and photodetectors (PDs) fabrication, packaging, and their characterization. His current main research includes the study and realization of stable high power deep UV light-emitting diodes lamp for their high power applications.

Hwu, Jenn-Gwo (EL.6)
Jenn-Gwo Hwu was born in Tainan, Taiwan, Republic of China, on August 29, 1955. He received the B.S. degree in electronic engineering from National Chiao-Tung University, Republic of China, in 1977 and the M.S. and Ph.D. degrees in electrical engineering from National Taiwan University, Republic of China, in 1979 and 1985, respectively. He joined the faculty of National Taiwan University in 1981. Presently, he is a Professor in the Department of Electrical Engineering and the Graduate Institute of Electronics Engineering, National Taiwan University.

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Takashi Ide received the B.E. (1986) and M.S. (1988) degrees in applied physics from Waseda University, Japan. He joined NEC Corporation in 1988, and has been working on the investigation of semiconductor surfaces using Scanning Tunneling Microscopy. Since 2002, He is currently working on the physical analysis of LSI devices in NEC Electronics Corporation.

Ielmini, Daniele (2B.1, 2E.1)
Daniele Ielmini was born in 1970. He received the Laurea (cum laude) and the Ph.D. degrees in Nuclear Engineering from the Politecnico di Milano, Milano, Italy in 1995 and 1999, respectively. In 1999, he joined the Dipartimento di Elettronica e Informazione, Politecnico di Milano, where he became an Assistant Professor in 2002. In 2006 he was a Visiting Scientist at Intel Co., Santa Clara and the Center for Integrated Systems (CIS), Stanford University, Stanford, USA. His research interest includes the modelling and characterization of Flash and post-Flash non volatile memories, such as nanocrystal memories, nitride-trap memories, chalcogenide-based phase-change memories (PCM) and resistive-switching memories (RRAM). He is author/coauthor of one book chapter and more than

120 papers published in international journals and presented in international conferences. He has been serving as a member of Technical Sub-Committees of international conferences, such as the IEEE-International Reliability Physics Symposium (IRPS, 2005-2008), the Semiconductor Interface Specialist Conference (SISC, 2008-2009) and the International Electron Device Meeting (IEDM, 2008-2009). He received the Impressive Award at E\PCOS 2007. He is a member of IEEE and MRS.

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Noriyuki Iguchi graduated from NEC Industrial Technology Junior College, Japan in 1990. In 1990, he joined Fundamental Research Laboratories, NEC Corp., Japan, where he was engaged in research and development nanometer-electron devices and nano-structured biochips. He has been engaged in research and development of solid-electrolyte nanometer switch. He is currently with Nano Electronics Res. Labs. of NEC Corp.

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Hideto Imai received the B.E. (1992), the M.E. (1994) and the Ph. D (1997) in materials engineering from Kyoto Univ. After joining NEC corp., Japan, in 1997, he has been worked on the development of characterization methods using synchrotron radiation x-rays, nuclear magnetic resonance spectroscopy and scanning probe microscope, in Nano Electronics Res. Labs. of NEC Corp.

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Kenji Imanishi was born in Nara, Japan, in 1963. He received the B.E. and M.E. degrees in electronic engineering from Osaka university, Osaka, Japan, in 1986 and 1988, respectively. In 1988, he joined the Fujitsu Laboratories Ltd., Kanagawa, Japan, where he has been engaged in research and development of compound semiconductor devices (HEMTs, HBTs) and their materials. Mr. Imanishi is a member of the Japan Society of Applied Physics.

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Tsutomu Imoto received the B.E. and M.E. degrees in electrical and electronics engineering from Sophia University, Tokyo, Japan, in 1987, 1989, respectively. In 1989, he joined Sony Corporation, where, at the Sony Research Center, Yokohama, Japan, he became involved in GaAs HEMT MMIC process/device development. From 1992 to 2000, he worked on GaAs JFET MMIC process/device development. From 2001 to 2003, he involved in research in organic molecular devices at the Fusion Domain Laboratory, Haneda, Tokyo, Japan. He is currently working on developing power MOS devices and their TCAD design platforms at Atsugi Technology Center, Kanagawa, Japan.

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Yusuke Inoue received the B.S. degree in physics and the M.E. degree in applied physics from Tokyo University, Tokyo, Japan, in 2000 and 2002.He is currently a member of the Advanced Devices Lab., Fujitsu Laboratories Ltd., Atsugi, Japan. In 2002, he joined Fujitsu Laboratories Ltd., Kanagawa, Japan, where he is engaged in development of microwave integrated circuits and high-speed compound semiconductor devices (high electron mobility transistors). Mr. Inoue is a member of the Institute of Electronics, Information and Communication Engineers, Japan.

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Siddarth Krishnan was born in Madras, India in 1978. He earned a bachelors degree in Materials Science (1999) at the Indian Institute of Technology (IIT), before moving to the United States where he received a master's degree in Materials Science at the University of Texas at Austin in 2001. He continued researching device and material properties of advanced gate materials at the same university, for which he was awarded a Ph.D in Electrical Engineering in 2005. He then researched high-k materials and gate electrodes and their long term reliability, for logic and memory applications, as a post-doctoral fellow, at SEMATECH, in Austin, Texas (2006). Since October 2006, he has been working with Semiconductor Research and Development Co-operative, at IBM, in East Fishkill, NY. During this time, his efforts have focussed around Unit Process, Process Integration, Device Physics and Reliability of Advanced gate dielectrics and metal electrodes, for logic and memory applications. Siddarth has co-authored over 30 conference and journal publications and has been awarded 4 patents, as a co-inventor. Siddarth is currently serving as the Vice-Chairman of the technical committee of International Reliability Physics Symposium, 2009 (IRPS), to be held at Montreal, Canda.

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Robert Laibowitz received a bachelors and masters degree from Columbia University and a Ph.D. degree in Applied Physics from Cornell University in 1967. He worked at the IBM Research Div. on tunnel junctions, superconductivity and dielectric measurements. He worked on the Josephson Computer project during 1974-1976 at the IBM Zurich Laboratory. He joined the EE Dept at Columbia in 2002 as a Senior Research Scientist and Adjunct Professor. His current work concerns leakage, trapping and reliability in low k dielectrics. He also consults on aspects of quantum computing at IBM. He is a Senior Member of the IEEE and a Fellow of the American Physical Society.

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Dean Lewis was born in 1965 in France. He is Professor at the University of Bordeaux where he teaches electronics. In 1996 he obtained a PhD degree concerning thermal characterization of integrated circuits using a laser beam. In 1997, he joined the IMS laboratory to develop new pulsed laser methodologies for ICs analysis and test. He is in charge of the ICs test and analysis team, which uses the ATLAS platform facilities. The first application concerns radiation sensitivity evaluation of ICs. The second application consists to develop defect localization techniques and the third one concerns dynamic fault injection.

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Sang Wook Lim received the B.S. degree in metallurgical engineering in 2002 from Yonsei University, South Korea, and M.S. degree in materials science and engineering from Stanford University in 2005. He joined the Memory Division of Samsung Electronics, Ltd., Gyeonggi-Do, Korea. He has been working on the process development of sub-30nm NAND flash memories. His research interests include cell structure design, cell reliability such as endurance and data retention, and thin film properties of high-k materials.

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Seung-Hyun Lim received the B.S., M.S., Ph. D. degrees in material science and engineering from Seoul National University, Korea, in 1996, 1998, 2003, respectively. In 2003, he joined Samsung Electronics Company, Ltd., Gyunggi-Do, Korea. He has been engaged in the research and development of NAND Flash process technology. His research interests include thin oxide/dielectric technology and flash cell reliability.

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Barry P. Linder (M'89) received his B.S. from Pennsylvania State University in 1993, and an M.S and Ph.D. in electrical engineering from the University of California at Berkeley in 1999. His doctoral thesis dealt with plasma processing, plasma implantation, and plasma charging damage. Since graduation Dr. Linder has been employed as a Research Staff Member at the IBM T. J. Watson Research Center, Yorktown Heights, NY. Initially his work centered on the breakdown of ultra-thin gate oxides, including the statistics of breakdown phenomenon, post-breakdown conduction mechanisms, and the interaction between oxide breakdown and circuit operation. This work formed the basis for the paper that received "Outstanding Paper Award" at the 2003 International Reliability Physics Symposium. After 2003 his focus changed to electrical characterization and integration of metal gates and high-k materials. More recently he has concentrated on all reliability aspects of high-k/metal gate stacks with emphasis on dielectric breakdown and bias temperature instability.

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Juin J. Liou received the B.S. (honors), M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1982, 1983, and 1987, respectively. In 1987, he joined the Department of Electrical and Computer Engineering at the University of Central Florida, Orlando, Florida where he is now a Professor. His current research interests are cro/nanoelectronics computer-aided design, RF device modeling and simulation, and electrostatic discharge (ESD) protection design and simulation.

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Bin Liu received the B.Eng. degree in electrical engineering from the National University of Singapore (NUS) in 2008. Currently he is working toward the Ph.D. degree at the Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, NUS. His research interests include strained-silicon MOSFETs and reliability physics of CMOS device.

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Ziyuan Liu received the B. S. (1982) and the M. S. (1985) in Materials science and engineering from Beijing Institute of Aeronautics, Beijing, China, and the Dr. Sc. (1994) in Material Science from Tokyo institute of Technology, Tokyo, Japan. From 1996 to 1997, she worked as a frontier researcher in RIKEN (The Institute of Physical and Chemical Research). Since 1997 she joined NEC Corporation, where she was engaged in the development of device analysis technology. She is currently working on the development of FLASH memory reliability in NEC Electronics Corporation.

Lloyd, Jim (6A.1, IC.10)
Jim Lloyd was, for many years, a researcher into failure due to electromigration and recently interlevel TDDB. After graduating from Stevens Institute of Technology with a PhD in Materials Science in 1978, he worked at IBM, DEC, Max Planck Institut, his own consulting firm, JPL, back to IBM and now at SUNY Albany at the CNSE. Published over 100 papers and presented dozens of lectures and courses all over the world. Also flies airplanes and is a locally recognized sculptor.

Lo, Vui-Lip (BD.3)
Vui-Lip Lo received his Bachelor of Science degree (2001) in computer and electrical engineering from the Ohio State University, USA, and his Master of Science degree (2002) in control and automation from the Nanyang Technological University (NTU), Singapore. Moreover, V. L. Lo is going to receive his Ph.D. degree from NTU in July 2009. He is currently the member of IEEE. His research area is the theoretical study of breakdown in ultrathin gate dielectrics in nano-scale MOSFETs. Since 2008, V. L. Lo is working as a Senior Engineer in Chartered Semiconductor Manufacturing, Singapore, and his job responsibilities mainly involve the process integration of 45LP logic and SRAM devices.

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Melina Lofrano received the BSc degree in Physics in 2001 and the MSc in Mechanical Engineering in 2003 at the University of São Paulo, Brazil. From 2003 until 2006 she worked in research and product development, where she was responsible for the mechanical modeling and analysis. From 2006 she was involved with several

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Rathnait Long graduated from University College Cork, Ireland, with a Bachelors Degree in Electrical and Electronic Engineering in 2003. She completed her Research Masters in Microelectronic Engineering in Tyndall National Institute in 2005. Rathnait then worked in Analog Devices in Limerick, Ireland. She worked in the Yield Group, which was part of the Fabrication Engineering Technology Department. Rathnait began her PhD with Dr. Paul Hurley in October 2006, working on the high-k/III-V system of ALD deposited insulators on InGaAs. In May 2008, Rathnait was awarded the Fulbright - Enterprise Ireland Award in Science, Technology and Innovation to spend 8 months in Stanford University, California, with Professor Paul McIntyre. Rathnait was awarded 'Best Postgraduate Presentation' at Intel's European Research and Innovation Conference, Ireland, in September 2008.

Lossy, Richard (2C.2)
Richard Lossy received his diploma in physics from Düsseldorf University and his Dr.-Ing. in electrical engineering from the University of Wuppertal, both Germany. At the IBM Research Center, Yorktown Heights, USA, he worked on the deposition and properties of diamond thin films. Wide bandgap materials remained in the focus at Technical University Berlin, where silicon carbide semiconductors were exploited for the development of sensor devices. Now at Ferdinand-Braun-Institut, Berlin, activities are directed towards HEMT devices from wide bandgap gallium nitride for microwave power transistors.

Loveless, T. Daniel (2H.2)
Daniel Loveless received the B.S.E.E. degree from Georgia Institute of Technology in 2004 and the M.S.E.E degree from Vanderbilt University in 2007. He is currently pursuing a Ph.D. in electrical engineering in the Radiation Effects and Reliability group at Vanderbilt, where his work has included the design of single-event-hardened phase-locked-loops and the analysis of high-speed analog circuits in radiation environments. His research interests include CMOS, mixed-signal circuit design, and radiation effects in microelectronics. Mr. Loveless was awarded the Georgia Tech Alumni Association Scholarship from 2000 to 2004 and received the IEEE Nuclear Plasma and Sciences Graduate Scholarship in 2008.

Lowder, Jonathan (2D.1)
Jonathan E. Lowder will receive his B.S. in Electrical Engineering from the University of South Carolina, Columbia, in 2009. He has been an undergraduate researcher in the Photonics and Microelectronics Laboratory, University of South Carolina, for four years. His research interests include fabrication and characterization III-V nitride based devices. After his undergraduate degree, Jonathan plans to pursue a Ph.D. in III-V based devices and materials.

Lu, Chih-Yuan (3C.4, 3C.5, MY.1, MY.2, MY.4)
Chih-Yuan Lu received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1972, and the Ph.D. degree in physics from Columbia University, New York, NY, in 1977. He was a Professor with National Chiao-Tung University and was with AT&T Bell Laboratories from 1984 to 1989. He later joined the Electronics Research and Service Organization/Industrial Technology Research Institute (ERSO/ITRI), Hsinchu, Taiwan, as a Deputy General Director, responsible for the MOEA Grand Submicron Project, in 1989. This project successfully developed Taiwan's first 8-in manufacturing technology with high-density DRAM/SRAM. In 1994, he became the Cofounder of the Vanguard International Semiconductor Corporation, which is a spin-off memory IC Company from ITRI's Submicron Project. He was the VP of Operation, the VP of R&D, and later the President from 1994 to 1999. He is currently the Chairman and CEO of Ardentec Corporation, a VLSI testing service company. He also serves as President of Macronix International Company, Ltd. (MXIC), Hsinchu. He led the MXIC's technology development team to successfully achieve the state-of-the-art nonvolatile-memory technology. He has published more than 200 papers and has been granted 133 international patents. Dr. Lu was elected as a Fellow of IEEE and the American Physical Society. He is the recipient of the highest honor—the National Science and Technology Achievement Award by the Prime Minister of R. O. C.—due to his leadership and achievement in this Submicron Project. He is also the recipient of the IEEE Millennium Medal, and the most prestigious semiconductor R&D Award in Taiwan, from Pan Wen Yuan Foundation.

Lu, Chi-Pin (MY.2)
Chi-Pin Lu was born in Hsinchu, Taiwan, R.O.C., in 1978. He received the B.S. degree in mechanical engineering from the National Central University, Taoyuan, Taiwan, in 2001, and the M.S. degree in material science and engineering from the National Tsing Hua University, Hsinchu, Taiwan, in 2003. Since 2003, he has been with the Technology Development Center, Macronix International Company, Ltd., Hsinchu, where his current works are engaged in advanced diffusion module process development as well as the dielectric characteristics studies of the nitride-trapping non-volatile memories.

Lu, Minhua (2F.3)
Minhua Lu received Ph. D in physics from Case Western Reserve University in 1992. In 1995, she joined IBM T. J. Watson Research Center as a Research Staff Member and worked on liquid crystal displays. In 2003, she received IBM outstanding technical achievement award. Since summer 2006, her main focus is on Pb-free solder electromigrations. She holds 35 US patents and has over 50 publications.

Lu, Wen-Pin (MY.4)
Wen-Pin Lu was born in I-Lan, Taiwan, R.O.C. on December 20, 1967. He received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. in 1990 and the M.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C. in 1992. He joined Macronix International Co., Ltd., Hsinchu, Taiwan, in 1994 as a device engineer. From 1994 to 1999, he has worked on device analysis of non-volatile memory, especially in floating-gate flash memory. Since 2000, he has been engaged in the development of PACAND Flash memory technology, and has accomplished 0.18mm and 0.15mm of delivering. He is presently responsible for the Nitrite-based NBit technology and also floating gate NOR flash development at Macronix.

Lue, Hang-Ting (3C.4, MY.1, MY.2)
Hang-Ting Lue was born in Hsinchu, Taiwan in 1975. He received his B.S and M.S degrees in physics from National Tsing-Hua University (NTHU) in 1997 and 1999, respectively, and Ph.D. degree in electrical engineering from National Chiao-Tung University (NCTU) in 2002. He joined Emerging Central Lab. (ECL) in Macronix International (MXIC) in 2003. Currently he is the department manager of nano-technology R&D, and leads a team to develop advanced Flash Memory devices, and the related theoretical modeling and reliability physics. One of his famous inventions is "bandgap engineered SONOS" (BE-SONOS), which solves the fundamental problems of SONOS, providing both efficient hole tunneling erase as well as good data retention. From 2004 he has published more than 20 papers in the premier semiconductor conferences including IEDM, Symposium in VLSI Technology and IRPS, and a total of more than 60 technical papers in IEEE journal/letter/conference. He has received the prestigious Outstanding Young Innovator Award from Taiwan's Ministry of Economic Affairs in 2007. Currently he serves in the program committees of VLSI-TSA since 2007, and IRPS since 2008.

M, Siva Theja (3C.6)
Siva Theja M is pursuing B. Tech. and M. Tech. combined degrees from Electrical Engineering department of the Indian Institute of Technology (IIT) Bombay, since 2004. His research interests include semiconductor device modeling and simulation. He is currently working on metal nanocrystal based non-volatile memories.

Ma, Huan-Chi (2B.4)
Huan-Chi Ma was born in Tainan, Taiwan, R.O.C., in 1981. He received the B.S. and M.S. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2003 and 2005, respectively, where he is currently working toward the Ph.D. degree. His research interests include negative bias temperature instability degradation, nonvolatile memory reliability issues, and flicker noise characterization.

Madan, Anuj (CR.1)
Anuj Madan received his M.S. in Electrical Engineering from the Georgia Institute of Technology in 2008, and completed his B.E. in Electronics Engineering from Punjab Engineering College, India in 2006. He spent the summer of 2008 at IBM Essex Junction, developing thin-film SOI technology for power applications. He is currently a Ph.D. student in SiGe Devices and Circuits Team at the Georgia Institute of Technology. His research interests center around design and reliability of high dynamic range and high-power RF circuits using silicon/silicon-germanium. He was the recipient of IEEE Electron Devices Society Masters Fellowship in 2007 and Best Student Paper award at ISTDM in 2008.

Mahapatra, Souvik (3C.6)
Souvik Mahapatra received his PhD in Electrical Engineering from the Indian Institute of Technology (IIT) Bombay, India, in 1999. He was at Bell Laboratories, Murray Hill, NJ, USA during 2000-2001. Since 2002 he is with the Department of Electrical Engineering, IIT Bombay, India, and presently holds the position of Associate Professor. His research interests are in the area of characterization, modeling and simulation of CMOS and Flash memory devices, and device reliability. He has published more than 75 papers in peer reviewed journals and conferences, delivered invited talks at leading international conferences in the USA, Europe and Asia-pacific including at the IEEE IEDM, delivered reliability tutorials at the IEEE IRPS, and acted as a reviewer of several international journals and conferences. He also holds an honorary graduate faculty position at Purdue University, USA, and is a distinguished lecturer and senior member of the IEEE.

Makabe, Mariko (MY.7)
Mariko Makabe received the B.S. (1990), and the M.S. (1992) in physics from Tokyo University of Science, Japan. Since 1992 she has been engaged in development and manufacturing.

Makino, Takahiro (2G.2)
Takahiro Makino was born in Akita, Japan in 1980. He received the B.S. degree in physics from Gakushuin University, Tokyo, Japan, in 2004, and the M.S. degree in quantum science and energy engineering from Tohoku University, Miyagi, Japan, in 2006. From April 2006 he has been a Ph.D student in Department of Space and Astronautical Science, School of Physical Science, The Graduate University for Advanced Studies, Kanagawa, Japan. Takahiro Makino is a member of IEEE Nuclear and Plasma Sciences Society (NPSS).

Makiyama, Kozo (2C.1)
Kozo Makiyama was born in Yamaguchi, Japan, in 1962. He received the B.E. and M.E. degrees in electrical engineering from Osaka Institute of Technology, Osaka, Japan, in 1986 and 1988, respectively. In 1988, he joined Compound Semiconductor Laboratory in Fujitsu Laboratories, Ltd., Atsugi, Japan, where he has been engaged in research and development of HEMT technologies. Mr. Makiyama is a member of the Japan Society of Applied Physics.

Malandruccolo, Vezio (5F.1)
Vezio Malandruccolo received his MSc with honors in electronic engineering, from the University of Rome "La Sapienza", in 2004, with a thesis on Short Range Radar Sensor for automotive applications in conjunction with ST Microelectronics. In 2005, he joined ANSOFT as a specialist of high frequency simulation tools. From 2006 to 2007 he was in Infineon Technologies, Villach, Austria, where he worked on the design and simulation of mixed signal circuits for telecommunications products. Currently, he is working towards his Ph.D. at the ETH Zurich. His research interests include the realization of theoretical and experimental tools for the implementation of built-in reliability program, mainly based on in-situ reliability monitors, and indicators.

Malobabic, Slavica (5F.3, EL.5)
Slavica Malobabic received the Professional Electronics Engineer Degree in 2005 and the M.E. degree from Universidad Simon Bolivar, Caracas, Venezuela in 2006 and an M.S. at University of Central Florida (UCF), Orlando, Florida in 2008. She is currently pursuing PhD degree in Electrical Engineering at the University of Central Florida in Electrostatic Discharge (ESD) area. She has coauthored 3 articles in specialized technical journals, and 7 in international conferences. She received the IEEE Electron Devices Society's 2005 Region 9 Outstanding Student Paper award.

Manigrasso, Mariaflavia (2B.1)
Mariaflavia Manigrasso was born in 1984 in Taranto, Italy. She received the Laurea (Master) Degree in Electronic Engineering from Politecnico di Milano, Italy, in 2008. From 2007 to 2008 she worked on her thesis activity at Numonyx R2 Technology Center - Agrate Brianza (Italy), within Compact Model Team, focusing on NBTI characterization and modeling in 90 nm technology. During the same period she also collaborated with ST Reliability and Standard Library Validation teams. Since October 2008 she is with ST Communication Infrastructure Division as Design Engineer. Her interests are in the field of semiconductor device physics and technology.

Marathe, Amit (5B.2)
Amit P. Marathe earned his M.S. and Ph.D. in Materials Science and Engineering from the University of California, Berkeley in May 1991 and August 1996 respectively. His research work was in the field of high temperature superconductor thin film processes for integrated circuits with emphasis on high-Tc SQUIDs and Josephson Junctions. After graduating from Berkeley, he joined Analog Devices, Inc. in Santa Clara, CA where he was working on the process development and integration of BiCMOS Integrated circuits technology for over a year. Since joining AMD in Sunnyvale CA in October of 1997, he has led the reliability development of interconnect metallization for AMD's memory and microprocessor technologies. Currently, he is the Department Manager of the Technology Reliability Development Group at GLOBALFOUNDRIES. His group is involved with development of reliability methodologies and modeling failure mechanisms of ultra thin gate dielectrics, advanced transistor structures as well as Cu/low-k metallization. He has co-authored over 40 technical research publications. He is also a co-inventor of over 15 patents granted and over 50 pending US patents in the area of technology & reliability development.

Marino, Fabio Alessio (CD.4)
Fabio Alessio Marino was born in Catania, Italy, in 1982 and received the degree in Electronic Engineering from the University of Padova (Italy) on July 2006. In January 2006 he started a PhD in Information Engineering at the University of Padova. In 2008 he joined the Department of Computer Science of the Arizona State University, as a Graduate Research assistant. His reasearch interests are currently focused on Monte Carlo simulation of GaN HEMTs.

Martin, Thomas (2D.7)
Thomas Martin is a Ph.D. candidate at the University of Maryland. He is also the Director of Electrical Engineering and Product Assurance at L-3 Communications Display Systems. L-3 Communications is a member of the FlexTech Alliance as well as an industry partner with the Flexible Display Center in Tempe,AZ.

Martin-Martinez, Javier (2B.5)
Javier Martin-Martinez was graduated in Physics in 2004 at the Universidad de Zaragoza, Spain. He has collaborated with the Electronic Department of Universidad de Zaragoza investigating algorithms of learning for neuronal networks. At the moment, he is a PhD student in Universitat Autònoma de Barcelona (UAB), where his research is focused on the failure mechanisms in MOSFETs and their impact on circuits. During his PhD he has stay in Università degli Studi di Padova (Italy) and IMEC (Belgium) where he has work on electrical modelling for NBTI and dielectric breakdown.

Masada, Akiko (4A.2, 4A.4)
Akiko Masada received the B.S. and M.S. degrees in applied physics from the University of Tokyo, Tokyo, Japan, in 2005 and 2007, respectively. In 2007, she joined the Corporate Research and Development Center of Toshiba Corporation, Kawasaki, Japan, where she has been engaged in the research on reliability of MISFET with high-k gate dielectrics.

Massengill, Lloyd W. (2H.2)
Lloyd W. Massengill (S'80-M'87-SM'01-F'05) received the Ph.D. degree in Solid State Circuits from North Carolina State University in 1987. He now serves as Professor of Electrical Engineering at Vanderbilt University in Nashville, TN, where he teaches microelectronic circuit analysis and design, and studies radiation effects on integrated circuits. He also serves as Director of Engineering for the Vanderbilt Institute for Space and Defense Electronics. He has been guest editor for the IEEE Transactions on Nuclear Science, general chairman for the IEEE Nuclear and Space Radiation Effects Conference, and Associate Editor for the IEEE Sensors Journal. He is a Fellow of the IEEE.

Masuduzzaman, Muhammad (2A.4)
Muhammad Masuduzzaman received the B.S. degree in Electrical and Electronic Engineering (EEE) from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 2004. During 2005-2006, he worked as a Lecturer in the Department of EEE, BUET. He is currently enrolled in direct Ph.D. program at the Department of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA. His research interest includes physics, simulation and characterization of nanoscale devices. Currently he is working with reliability issues in high-κ devices.

Matsukawa, Shinji (EL.4)
Shinji Matsukawa was born in Hyogo, Japan, on October 3, 1973. He received the B.S. and M.S. degrees in applied physics from Osaka University, Osaka, in 1996 and 1998, respectively. In 1998, he joined the Analysis Technology Research Center, Sumitomo Electric Industries, Ltd., Itami, Japan, where he has been engaged in research and development of nano-scale analysis of compound semiconductor materials and devices. He is a member of the Japan Society of Applied Physics.

Matthews, David (2H.1)
David C. Matthews received the B.A. mathematics from Doane College, Crete Nebraska, the B.S. electrical engineering from Washington University, St. Louis Missouri, and the M.S. electrical engineering from Iowa State University, Ames, Iowa, in 1984, 1985, and 1994, respectively. He is currently a Ph.D. student at the University of Iowa, Iowa City, Iowa. He has developed avionics for Rockwell Collins, Cedar Rapids, Iowa since 1985. He is also an adjunct professor in the department of Electrical and Computer Engineering at the University of Iowa, where his research interests include reliable computing and soft errors.

Matzner, Christian (3F.1)
Christian Matzner was born in Eichstätt in 1980. After he received the diploma degree in mechatronics at the university of Erlangen-Nuremberg he started as a doctorand in a exploratory cooperation between the University of Erlangen-Nuremberg and the Audi AG Ingolstadt. In his postgradute research, the influence of humidity and dew condensation on electronic systems is being investigated. His reseerach and development efforts are focusing on humidity and condensation testing, reliability assurance and automotive mission profiles.

Mawatari, Kouzou (6C.2)
Kouzou Mawatari received the M.E. degree from Kyushu University, Fukuoka, Japan, in 1991. In the same year, he joined Sony Corporation, Atsugi, Kanagawa, Japan, where he has been engaged in the design of mixed signal LSI and ESD protection technology.

McLain, Michael (2G.4)
Michael L. McLain graduated with a B.S. degree in Electrical Engineering and a minor in Mathematics from the University of Arizona in 2004, and with a M.S. degree in Electrical Engineering from Arizona State University in 2006. He is currently pursuing a Ph.D. in Electrical Engineering at Arizona State University. His research focuses on testing, characterizing, and modeling hostile environment effects in semiconductor materials, devices, and integrated circuits.

McMorrow, Dale (2H.2)
Dale McMorrow received the B.S. in Chemistry from Spring Hill College, Mobile, AL, and the Ph.D. in Physical Chemistry from The Florida State University. He presently is head of the Radiation Effects Section at the Naval Research Laboratory. He has authored over 150 papers in refereed journals. He has served as Technical Chair for the Single-Event Effects Symposium, session chair at the IEEE Nuclear and Space Radiation Effects Conference (NSREC), the Radiation and its Effects on Components and Systems (RADECS) Conference, and the Single-Event Effects Symposium, won the 2003 NSREC best paper award, and has won three NRL Berman Awards for best paper.

Meneghesso, Gaudenzio (2D.3, 2D.5, 2D.6, CD.4, CD.5)
Gaudenzio Meneghesso, born in Padova, Italy in 1967. He graduated in Electronics Engineering at the University of Padova in 1992 and in 1997 he received the Ph.D. degree in Electrical and Telecommunication Engineering working on hot-electron characterization and reliability of GaAs-based and InP-based HEMT's and P-HEMT's. Since 2002 is Associate Professor at Padova University . His research interests are III-V, III-N semiconductor devices, RF-MEMS switches and ESD protection structures. He published over 300 technical papers (more than 30 Invited Papers, 4 best paper awards). He is Editor of the IEEE Electron Device Letter for the compound semiconductor devices area.

Meneghini, Matteo (2D.3, 2D.5, 2D.6, CD.5)
Matteo Meneghini received the degree in electronics engineering from the University of Padova, Italy, in 2004, and the PhD in Electronics and Telecommunication Engineering in 2008, working on the optimization of advanced optoelectronic devices based on compound and organic semiconductors. He is now Research Fellow at the Department of Information Engineering of the University of Padova. His main interest is the characterization, reliability and simulation of compound semiconductor and organic semiconductor devices..

Mikami, Nobukazu (SE.3)
Nobukazu Mikami received the B.S. (2003) the M.S. (2005) in faculty of industrial science and technology from Tokyo University of Science Japan. He joined Sony Corporation in 2005. He is a member of the Advanced Processor Department LSI Business Division Semiconductor Business Group. His current researches are cosmic ray-induced soft error in LSI.

Miranda, Enrique (BD.1)
Enrique Miranda obtained the PhD degrees in Electronics Engineering and Physics from Universitat Autònoma de Barcelona (UAB), Spain and Universidad de Buenos Aires (UBA), Argentina in 1999 and 2001, respectively. From 1987 to 2003, he was Associated Professor at the Faculty of Engineering-UBA and from 2001 to 2003, Associated Researcher at the National Council of Science and Technology, Argentina. Since 2004, he is Professor at the Escola Tècnica Superior d'Enginyeria-UAB. He has authored and co-authored more than 80 papers in international journals. Dr. Miranda serves as Editorial Advisor of Microelectronics Reliability and is member of the Distinguished Lecturer program of the IEEE-Electron Devices Society. He has served in the technical committees of INFOS'07&09 and IRPS'08&09. His research interests include dielectric physics and reliability.

Mitani, Yuichiro (4A.2, 4A.4)
Yuichiro Mitani, received the B. E. and M. E. in material science and engineering from Tohoku University, Sendai, Japan, in 1990 and 1992, respectively. He received the Ph.D. from the University of Tokyo in 2009.He joined the R&D Center, Toshiba Corporation in 1992. His primary works were concerned in the Si-CVD and the ultra-shallow junction process technology. Since 1999, he has been with the Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation, Yokohama, Japan. His present research interests and activities cover the ultra-thin oxide process technology and the study of the reliability of ultra-thin gate oxide layer (SiO2, SiON and High-k dielectrics) for ULSI technology. He serves (or served) on the technical committees of International Conference on IC Design & Technology (ICICDT) and IEEE International Reliability Physics Symposium (IRPS). He is a member of the Japan Society of Applied Physics.

Mitra, Subhasish (6B.4)
Subhasish Mitra is an Assistant Professor in the Departments of Electrical Engineering and Computer Science of Stanford University where he leads the Robust Systems Group. His research interests include: 1. robust system design, 2. VLSI design, CAD, validation, test, and 3. design for emerging nanotechnologies. Before joining Stanford, Prof. Mitra was a Principal Engineer at Intel. His major honors include the Presidential Early Career Award for Scientists and Engineers, CAREER Award, Terman Fellowship, IEEE Trans. CAD Best Paper Award, ACM SIGDA Outstanding New Faculty Award, Design Automation Conference Best Paper Award, and the Intel Achievement Award, Intel's highest corporate honor.

Miura, Hideo (4A.6)
Dr. Hideo Miura received M.S. and Ph.D degrees from Tohoku University in 1983 and 1992, respectively. He has been working on the mechanical reliability of nano-scale materials, thin film devices, electronic packaging and modules in Hitachi Ltd. from 1983-2003. Now he is Professor of Fracture and Reliability Research Institute, Graduate School of Engineering, Tohoku University.

Miyazaki, Hiroshi (IC.2)
Hiroshi Miyazaki received the B.S. (1982), the M.S. (1984) and the Dr.,Eng. (1998) in chemical engineering from Kyoto University, Japan. Since 2003 he has been working for the Process Development Dept., Renesas Technology Corp., on process development. He is currently working on BEOL process integration including interconnect reliability issues.

Mizuno, Masayuki (6B.4)
Masayuki Mizuno received the B.S., M.S., and Dr.Eng. degrees in electronic engineering from Osaka University, Japan, in 1991, 1993, and 2000, respectively. In 1993 he joined NEC Corporation, where he has been engaged in the research and development of low-power circuit techniques, world's first single-chip MPEG2 video encoder LSIs, high-speed clock generation circuits and distribution networks especially for NEC's supercomputers, and high-bandwidth serial links. During a leave from 1999 to 2000 he engaged in the research of interconnection network for chip multiprocessors at Stanford University as a visiting scholar. Currently he is a senior manager of Device Platforms Research Laboratories, NEC Corporation, and his research interests lie in dependable LSI design and test, low-power PAN & BAN wireless and high-speed wireline communications. He was a member of MIRAI and a Visiting Professor at Hiroshima University, Japan. He is a member of IEEE and IEICE and the program chair of 2009 Symposium on VLSI Circuit.

Moe, Craig (2D.2)
Craig Moe received the B.S. degree in applied science from the University of North Carolina in 1998 and the Ph.D. in materials from the University of California at Santa Barbara in 2007. He is currently joint post-doctoral candidate with the Army Research Laboratory and Boston University under Dr. Ted Moustakas. His research is primarily focused on the growth and fabrication of AlGaN and AlN-based optoelectronic devices.

Moens, Peter (4C.2)
Peter Moens received a M.Sc. and a Ph.D. in solid state physics from the University of Gent, Belgium, in 1990 and 1993 respectively. From 1993 till 1996, he worked as a post-doctoral fellow in collaboration with Agfa-Gevaert. In 1996, he joined ON Semiconductor where he is involved in the power device development. He authored over 100 papers in international scientific journals and conference proceedings, and holds several patents. Dr. Moens is member of the technical program committee of ISPSD, IRPS and the ESD/EOS Symposium, and serves as the chair of the HV reliability subcommittee of IRPS. He also serves as the technical program chair of ISPSD2009.

Mokrani, Arezki (EX.1)
Arezki Mokrani was preparing his Master. degree in Microelectronics at Microelectronics and Nanotechnology Division, of CDTA, Algiers, Algerea.

Monaghan, Scott (BD.1)
Scott Monaghan obtained his PhD in 2007 from University College Cork, Ireland while researching the interfacial properties of hafnium-based silicates with silicon at Tyndall National Institute. This work focused on atomic-scale characterization of possible interfacial configurations and the early stage growth mechanisms for silicon oxide interfacial layers. Since 2007 he has been developing systematic techniques utilizing experimental measurement and theoretical modeling to extract electrical and physical properties of both the high-k dielectric layer and the lower-k interfacial layer formed at the silicon or III-V compound semiconductor surface. Dr Monaghan's research experience with bulk and interfacial properties of dielectric and semiconductor materials is a key ingredient for developing and characterizing alternative high-k dielectrics on present silicon-based semiconductor substrates and high mobility III-V compound semiconductor substrates that by necessity also employ metal gate electrodes

Mongeon, Stephen (5B.1)
Stephen Mongeon received his B.S. and M.S. degrees from the University of Vermont in 1978 and 1980 respectively. He joined IBM at the Burlington, Vermont Semiconductor Fab in 1982 where he is currently employed as an Advisory Engineer in a Physical Failure Analysis laboratory.

Monzio Compagnoni, Christian (3C.1)
Christian Monzio Compagnoni was born in Busto Arsizio, Italy, in 1976. He received the Laurea (cum laude) degree in Electronics Engineering and the Ph.D. degree in Information Technology from the Politecnico di Milano, Milan, Italy, in 2001 and 2005, respectively. Since 2002 he has been with the Dipartimento di Elettronica e Informazione (DEI), Politecnico di Milano, where he became an Assistant Professor in 2006. His research activities include characterization and modeling of advanced non-volatile memories and MOS devices. In 2009 he has been serving as member of the memory committee of the IRPS conference.

Moon, Joo-Tae (3C.2, 3C.3, IC.5)
Joo-Tae Moon is the vice president and the head of process development team of Samsung Semiconductor R&D center.
Since joining Samsung Electronics Co., Ltd., Gyeonggi-Do, Korea, in 1989, he has developed semiconductor fabrication technologies (mainly lithography) of 64M, 256M, 1G, 4G, and 16G DRAM devices. His research interests include semiconductor device processing and fabrication, and of emerging technology for sub-30 nm memory devices. He received the B.S. degree in metallurgical engineering from Seoul National University, Seoul, Korea, in 1984, and the M.S. and Ph.D. degree in material engineering from KAIST, Daejon, Korea, in 1986 and 1989, respectively.

Moroz, Victor (AP.1)
Victor Moroz received his Ph.D. in Semiconductor Physics in 1992 from the University of Nizhny Novgorod. His professional career revolves around semiconductor physics and includes silicon process integration in the industry, teaching undergraduate and graduate students, and for the last 14 years - developing process simulation and DFM tools at TMA and TCAD Department at Synopsys. Several facets of this activity are reflected in a book and over 100 technical papers, invited presentations, and patents.

Morusupalli, Rao (FF.1)
Rao Morusupalli is a Technical Leader at Cisco Systems, San Jose, CA. He joined Cisco in 2006 and is working in the area of Semiconductor components technology and reliability. Prior to Cisco, Rao was employed with Intel Corporation, Santa Clara, where he worked on Cu Interconnect technology development and interconnect reliability for Intel's microprocessor and flash memory technologies. Rao Morusupalli has a graduate degree in Materials Science from Stanford University.

Mukhopadhyay, Gautam (3C.6)
Gautam Mukhopadhyay received M.Sc.(Physics), with 1st rank from IIT-Kharagpur, India (1966); BARC Training School (1967) with 2nd rank, Bombay, India; Ph.D.(1973) in Solid State Theory from Theory Group, Tata Institute of Fundamental Reasearch (TIFR), Bombay, India; International Atomic Energy Agency (IAEA) Fellow (Jan-July, 1973) at International Centre for Theoretical Physics (ICTP), Trieste, Italy; Visiting Scientist (March, 1973- September 1978) in Institute of Theoretical Physics, Chalmers University of Technology, Gothenburg, Sweden; Assistant Professor (1978-1987) at Physics Department, IIT-Bombay; Associate of ICTP, Trieste (1980-85); Senior Solid State Fellow (1985-87) at ICTP, Trieste, Italy; Professor of Physics (1987-) at IIT-Bombay. He has worked on various areas of Theoretical Condensed Matter Physics, like electronic energy band calculations for Ce, electron correlations for homogeneous and inhomogeneous electron systems, surface physics, Magnetism in Rare Earth Iron Garnets (RIG), optical properties of dielectric and magnetic nanoparticles, etc. He has more than 100 papers in peer reviewed journals and conference Proceedings.

Murakami, Eiichi (3E.1, BD.4)
Eiichi Murakami received the B.S./M.S./Ph.D. degree in applied physics from Waseda University, Tokyo, Japan, in 1981/1983/1995, respectively. He joined the Central Research Laboratory, Hitachi, Ltd. Japan, in 1983. He worked on Si-SPE, SiGe, ultrashallow-junction, and MOSFET's design & characterization studies. He is now the manager of Process & Device Analysis Engineering Development Department in Renesas Technology Corp. His current interest is in reliability and failure physics in Si-LSI. Dr. Murakami is a member of the Japan Society of Applied Physics and the IEEE EDS. He served as a sub-committee member of CMOS and Interconnect Reliability in IEDM 2004,05.

Murata, Naofumi (3E.1)
Naofumi Murata received the B.S. (1986) and the M.S. (1988) degrees in physics from Tokyo Institute of Technology, Tokyo, Japan. Since 1988 he has been working for the Process Technology Development Div., Renesas Technology Corp., on VLSI process and device analysis engineering development. He is currently engaged in failure analysis of ULSIs.

Na, Kwang Duck (XT.3)
Kwang Duck Na received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, in 2007 and 2009, respectively. He have focused on the fabrication of metal-oxide-semiconductor capacitor using ZnO as a transparent oxide semiconductor and HfO2 as a high-k material. Also he was dispatched to Korea Institute of Science and Technology (KIST) to study charge densities changes and vacancy formation energies of strained Ge using ab-initio calculation in 2008.

Nafría, Montserrat (XT.16)
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Sarah Armstrong Nation, an employee of NSWC Crane, is working as a PhD student at Vanderbilt University studying Electrical Engineering with an emphasis on radiation effects on electronics. Sarah graduated with a BSEE from Purdue University in 2001. She worked with Crane for five years as an analog IC designer, project lead, and a program manager before returning to full-time student status.

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Hiroyuki Nitta received the M.S. in aplied Physics from Tokyo Institute of Technology (1995). In 1995, he joined Semiconductor Technology Lab, Toshiba Corp., and engaged in development of DRAM device technologies. Since 2001, he has been working on Flash Memory Device Technology Dept.

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Nicolar Nolhier was born in Pau, France, in 1966. He received the Ph.D. degree in electronics from the National Institute of Applied Sciences (INSA), Toulouse, in 1992. He is Professor at the University Paul Sabatier, Toulouse, and has joined the Laboratoire d'Architecture et d'Analyse des Systèmes (LAAS-CNRS). Firstly motivated by Rapid Thermal Processing control and modeling, his interests moved in Power Devices design and simulations. In 1996 he initiated, in LAAS, the study of ESD protections using 2D electrothermal simulations, and investigated in TLP experiments. His now involved in System Level ESD protection strategy and MEMs reliability toward ESD events.

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Dr. Eugene Normand joined the Boeing Company in 1984 after 15 years in the nuclear power industry, having received his Ph.D. in nuclear engineering from the University of Washington in 1970. Initially he provided nuclear analysis support for various Boeing space and military airplane projects and served as Principal Investigator for the DOE Multimegawatt Space Nuclear Power program. On the Boeing 777 program he was the first to establish requirements to define/quantify the impact of atmospheric neutrons on avionics via single event effects (SEE). He led a joint NRL study with IBM that was the first to document the occurrence of single event upsets (SEUs) in-flight and demonstrate they were caused by the atmospheric neutrons. He has been involved in the writing of portions of all of the international standards devoted to the subject of neutron-induced single event effects, JESD89 and JESD89A for JEDEC and IEC TS 62396 Parts 1-5 for the IEC. Since its inception in 2001, he has been a key contributor to the work of the AVSI working group devoted to mitigating radiation effects on current and future avionics systems. He retired from Boeing in 2007 and returned later that year as a consultant. In 2008 he formed EN Associates to provide his expertise regarding single event effects from atmospheric neutrons to the avionics industry.

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Pascal Nsame is an active IBM professional, IEEE member, and STEM outreach volunteer. His is currently responsible for all aspects of semiconductor product quality from development through qualification and manufacturing as well as quality in the field at the System and Technology Group of IBM. He graduated from University of Quebec with a Bachelor of Science in Microelectronics and a Master of Science in Physics. In parallel, he pursued his Ph.D. thesis in Electrical Engineering. He started his microelectronics career in 1996 when he joined the Canadian Microelectronics Corporation as a CAD/CAE/System Design Engineer. He joined IBM in 1999 as an Engineer/Scientist where he has focused his interests and contributions on semiconductor products. He has authored and published 12 technical papers and holds 25 patents issued or pending.

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Toshinori Numata received BS, M.S., and Ph.D. degrees in electronic engineering from Osaka University, Japan, in 1995, 1997, and 2006. He joined the Corporate Research and Development Center, Toshiba Corporation, Japan, in 1997, where he has been engaged in the research of SOI devices. From 2001 to 2006, he was a member of MIRAI Project, ASET, where he worked on strained SOI MOSFETs. From 2006 to 2007, he was a Visiting Scholar at University of Florida, FL, where he studied strained Si technology. Since returning to Advanced LSI Technology laboratory, he has been engaged in the research on Si MOSFET.

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Anthony Oates received his B.S. (1982) and Ph.D. (1985) in physics from the University of Reading, U.K. He is presently responsible for reliability physics development at TSMC. Prior to joining TSMC in 2002, Dr. Oates spent 17 years as a distinguished member of the technical staff and technical manager at Bell Labs and Agere System, where he was responsible for reliability characterization and process qualification of CMOS technologies. Dr. Oates has over 80 publications and holds 4 patents. He is a frequent conference speaker and tutorial presenter. Dr. Oates has a long-standing involvement with the International Reliability Physics Symposium, serving as the general chair of the symposium in 2001. He is also currently Editor-in-Chief of the IEEE Transactions on Device and Materials Reliability, and has participated in the technical leadership of the International Electron Device Meeting (IEDM) and Materials Research Society (MRS) meetings.

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Dan O'Connell is Senior Process Engineer in the Central Fabrication group in Tyndall National Institute. He has a BSc. from the Open University and has studied Analogue and Digital Electronics, Physics and Inorganic Chemistry. He has worked at Tyndall since 1993 and has wide experience of all aspects of semi-conductor device fabrication including photo-lithography, wet etching, RIE/ICP etching, thin-film deposition including PECVD, sputtering and e-beam evaporation. He is currently involved in developing deposition and patterning techniques for e-beam evaporated dielectrics.

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Eamon O'Connor was born in Cork, Ireland in 1980. He received his B.E. in Electrical and Microelectronic Engineering from University College Cork in 2002. He was awarded an MEngSc in 2005 for research at the Tyndall Institute (University College Cork) on the fabrication and characterization of electroluminescent devices based on organic and inorganic materials. Since 2006 his research has been focused on the electrical characterisation of MOS device structures utilising high-k dielectric materials on high-mobility III-V compound semiconductors. He is currently a PhD student in the research group of Dr. Paul Hurley at the Tyndall Institute.

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Robert O'Connor received the B.S. in Applied Physics from Dublin City University (2001) and the Ph.D. from the same institution (2005). In 2006 he worked at Intel Ireland as a Process Engineer. He was awarded an EU Marie Curie Fellowship in 2006 to continue his research on the electrical characterisation of high-k gate dielectric layers at IMEC, Belgium. He is currently with the School of Physical Sciences at Dublin City University working on the growth of high-k dielectrics on III-V substrates.

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Kohji Ohgata received the B.S. (1990) in chemistry from Rikkyo Univ., Tokyo, Japan. In 1990, he joined Fujitsu Labs. Ltd., and engaged in research and development of a-Si and low-temperature poly-Si TFTs for LCD. Since 2001, he has been working on reliability of gate dielectrics for CMOS devices at Semiconductor Technology Development Division, Hitachi, Ltd., and now he is with Renesas Technology Corporation.

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Yuzuru Ohji received B.S. (1975) and M.S. (1977) degrees in metallurgy from the University of Tokyo, Tokyo, Japan. In 1977, he joined the Central Research Laboratory of Hitachi Ltd., Tokyo, where he has been doing research on metalization and reliability physics of thin dielectric films for MOS VLSI's. From 1996 to 1997, he engaged in developing thin tunneling oxide of Flash memory in Semiconductor and Integrated Circuits Division of Hitachi Ltd. From 1997 to 2000, joining Device Development Center of Hitachi Ltd., he developed fabrication process of Ta2O5 capacitor for high density DRAM's. From 2000 to 2003, he has been managing the development of device simulation technology, robust designing technology, reliability designing technology and physical analysis technology for VLSIs in Semiconductor and Integrated Circuits Division of Hitachi Ltd. From 2003 to 2006, he has been managing the Advanced Device Development Department of Renesas Technology Corp., where he has been developing advanced CMOS devices, advanced Flash memories, and next generation on chip non-volatile memories. Since 2006, joining Semiconductor Leading Edge Technologies, Inc. as an assignee of Renesas Technology Corp., he has been managing the development of front-end process and TCAD. Mr. Ohji is a member of IEEE.

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Toshihiro Ohki was born in Chiba, Japan, on August 7, 1976. He received the B.E. and M.E. degrees in electrical engineering from Waseda University, Tokyo, Japan, in 1999 and 2001, respectively. In 2001, he joined Fujitsu Laboratories Ltd., Atsugi, Japan, where he has been engaged in the research and development of InP-based RTD/HEMTs and GaN-based HEMTs for high-speed optical and wireless communication systems. Mr. Ohki is a member of the Japan Society of Applied Physics.

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Tadahiro Ohmi received the B.S., M.S., and Ph.D. degrees in electrical engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1961, 1963, and 1966, respectively. Prior to 1972, he served as a Research Associate in the Department of Electronics, Tokyo Institute of Technology, where he worked on Gunn diodes such as velocity overshoot phenomena, multivalley diffusion and frequency limitation of negative differential mobility due to an electron transfer in the multi-valleys, high-field transport in semiconductor such as unified theory of space-charge dynamics in negative differential mobility materials, Bloch-oscillation-induced, negative mobility and Bloch oscillators, and dynamics in injection lasers. In 1972, he moved to Tohoku University, Sendai, Japan, where he is currently a Professor at the New Industry Creation Hatchery Center. He is engaged in researches on high-performance ULSI such as ultrahigh-speed ULSI based on gas-isolated-interconnect metal-substrate SOI technology, base store image sensor (BASIS) and high-speed flat-panel display, and advanced semiconductor process technologies such as low kinetic-energy particle bombardment processes including high-quality oxidation, high-quality metallization, very-low-temperature Si epitaxy, and crystallinity-controlled film growth technologies from single-crystal, grain-size-controlled polysilicon and amorphous highly selective CVD, highly selective RIE, and high-quality ion implantation with low-temperature annealing capability based on ultraclean technology concept supported by newly developed ultraclean gas supply system, ultrahigh vacuum-compatible reaction chamber with self-cleaning function, and ultraclean wafer surface cleaning technology. His research activities are summarized by the publication of over 1300 original papers and the application of 1600 patents. Dr. Ohmi serves as the President of the Institute of Basic Semiconductor Technology-Development (Ultra Clean Society). He is a Fellow of the Institute of Electricity, Information and Communication Engineers of Japan. He is a member of the Institute of Electronics of Japan, the Japan Society of Applied physics, and the Electrochemical Society. He received the Ichimura Award in 1979, the Inoue Harushige Award in 1989, the Ichimura Prizes in Industry-Meritorious Achievement Prize in 1990, the Okouchi Memorial Technology Prize in 1991, the Minister of State for Science and Technology Award for the Promotion of Invention (the Invention Prize) in 1993, the IEICE Achievement Award in 1997, the Okouchi Memorial Technology Prize in 1999, the Werner Kern Award in 2001, the ECS Electronics Division Award, the Medal with Purple Ribbon from Government of Japan and the Best Collaboration Award (the Prime Minister's Award) in 2003.

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Piero Olivo is Full Professor of Electronics and Faculty Dean at the Engineering Faculty of the University of Ferrara, Italy. The scientific activity concerned several theoretical and experimental aspects of microelectronics, with emphasis on physics, reliability and characterization of electron devices and non volatile memories as well as design and test of integrated circuits. In particular he is coauthor of the first paper describing and analyzing Stress Induced Leakage Current (SILC) in thin oxides, presented at IRPS '87, and of the first analytical theory of aliasing error in Signature Analysis testing techniques.

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Kenji Orita (M'02) was born in Osaka, Japan in 1971. He received the B.S. and M. S. degrees in electronics engineering from Kyoto University in 1995 and 1997, respectively. In 1997, he joined Matsushita Electric Industrial Co., Ltd (Panasonic). His main research is developing light-emitting diodes (LEDs) and laser diodes based on GaAs and GaN, including photonic crystal LEDs. He is a member of IEEE/LEOS and the Japanese Society of Applied Physics (JSAP).

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Sean Joseph O'Shea is a Principle Scientist at IMRE, Singapore. He received his PhD (1990) in Physics from the University of Sydney, Australia and then worked in the Engineering Department, Cambridge, UK until moving to Singapore in 1998. His main research interests are scanning probe microscopy, MEMS, nanotechnology and biomedical sensors.

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Akira Oyama received the B.S. (1992) in information engineering from Sanno University, Japan. He joined Sony Corporation in 1992. He is a member of the Advanced Processor Department, LSI Business Division, Semiconductor Business Group. His interests are cosmic ray-induced soft error in LSI, reliability engineering of advanced CMOS logic, ESD and Latch up in LSI.

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Sangwoo Pae received a B.S.E.E. degree from the Chung-Ang University in Korea (1994) and M.S. and Ph.D. degrees in 1996 and 1999, respectively, in ECE from Purdue University in West Lafayette, IN, USA. He has been with Intel since 2000 in the Logic Technology and Development Quality and Reliability Group in Hillsboro, Oregon. He has contributed to the development and reliability of Intel's 130nm, 90nm, 65nm, 45nm and most recently on 32nm logic technology nodes and has received two Intel's highest achievement IAA awards. He is currently a Sr. Staff QRE. He has authored/co-authored over 25 publications and has 12 issued/pending patents in the field of process, circuits and reliability. His current research interests involve reliability issues and novel devices. He gave High-K and Metal Gate reliability tutorials/invited talks at IRPS/SICC and is Gate dielectric reliability program chair for the 2009 IRPS.

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S. Y. Pai received the B.S. (1970) in Physics from National Taiwan University, M.S. (1973) in Material Science and Ph.D. (1978) in Electrical Engineering, both from University of Minnesota. He is currently the Senior Director of Reliability at Xilinx, responsible for overall product reliability including qualification, reliability assurance and failure analysis. Prior to joining Xilinx in 2000, Dr. Pai worked at Cypress Semiconductor in technology developments involving bipolar, CMOS, BiCMOS and Non-Volatile processes from 1 micron to 0.18 micron. His primary interests are process integration, defect/outlier elimination and device/reliability modeling.

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Sagnik Pal received his B.Tech (Hons.) in electrical engineering from Indian Institute of Technology, Kharagpur in 2004. In 2006, he received his M.Tech (Hons.) in electrical engineering from Indian Institute of Technology, Kanpur. His M.Tech thesis dissertation was on optically actuated MEMS structures. He is currently pursuing his PhD at the University of Florida, Gainesville. He has published one journal paper and six conference papers. His research interests include reliability, modeling and fabrication of MEMS devices. He has a keen interest in electromagnetism and control theory.

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Luigi Pantisano received his MS and PhD degrees in electrical engineering from University of Padova, Padova, Italy, in 1996 and 2000, respectively. In 2000, he was with Bell Laboratories - Lucent Technologies, Murray Hill, NJ, pursuing the impact of plasma-charging damage on RF CMOS devices. Since 2001, Luigi joined IMEC to work on high-k gate dielectrics for CMOS and Memory technologies. Luigi is committee member of several conferences (SISC, IRPS, IGSAT, ICMTS) and contributed to more than 150 papers in the field of plasma damage, RF measurements, reliability and electrical characterization of novel high-k devices.

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Daniel Pantuso received a Ph.D. in Mechanical Engineering from MIT in 1997 with focus on applied mechanics and materials. He joined Intel in 1997 and has worked in the area of thermal management at system and interconnect level, interconnect reliability, sort/test integration and die/package interactions. He is currently a group leader in the thermal and thermo-mechanical areas in the process and technology modeling department. He has authored about 25 journal and conference papers and holds 2 US patents.

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George Papaioannou received the BSc degree in physics from University of Athens, the MSc degree from University College London, England, and the PhD degree in solid state physics from the University of Athens. In 1975 he joined the Physics Laboratory, Physics Department of University of Athens, as a research assistant and latter (1978) as a lecturer conducting research in III–V compound semiconductors, mainly in semi-insulating GaAs. In 1982 he joined the Solid State Physics Section at University of Athens where from 1982 he worked as a senior lecturer. Presently he is associate professor at the Solid State Physics Section of Athens University, leading a team on the transport properties and the radiation effects in compound semiconductors and III–V semiconductor devices and the interaction of light in III–V compound semiconductor and SOI structures and devices. Recently he is working on the investigation of polarization effects in insulating materials in RF-MEMS switches. He has been contributed to 70 publications and more than 130 conference presentations.

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Biju Parameshwaran is a Senior Member of Technical Staff in the Logic Technology Development division at Advanced Micro Devices. He received his B.Tech degree from the Indian Institute of Technology, Kharagpur in 1993, and M.S. in Materials Science & Engg. in 1995 from Arizona State University, Tempe, AZ. He joined Cypress Semiconductor in 1995. He has worked on and led development and transfer projects on various technologies including CMOS memory, non-volatile SONOS, BiCMOS SiGe, and Magnetic RAM development. He joined Advanced Micro Devices in 2005, functioning as a liaison between technology development, reliability, design and product engineering.

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Chan-Kwang Park (S'90-M'92) was born in Incheon, Korea, in 1961. He received the B.S. degree in electronic engineering from Sogang University, Seoul, Korea, in 1984. He received the M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of

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Jung Min Park received the B.S. degree in material science and engineering from Korea University, Seoul, in 2002 and the M.S. degree in material science and engineering from Gwangju Institute of Science and Technology (GIST), Gwangju, in 2004. He has been Engineer at Samsung electronics (SEC) since 2004 with responsibilities of high-k MIM capacitor such as eDRAM and Analog-RF capacitor and currently, metal gate process.

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Min-Sang Park received the B.S. (2005) in electronics engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea. He is currently in M.S. and Ph.D. integrative program course at POSTECH. His main research is related to CMOS devices.

Park, Tae Joo (XT.3)
Tae Joo Park received the B.S. and Ph. D. degree in Materials Science and Engineering from the Seoul National University, Seoul, Korea, in 2002 and 2008, respectively. His research at Seoul National University covered electrical and chemical characterizations of advanced gate stacks with metal gate/high-k/high mobility channel and non-volatile memory applications. Since November 2008, he has been a research scientist of the Materials Science and Engineering at University of Texas at Dallas where he is studying advanced nano-electronic devices based on organic/inorganic thin films.

Patel, Nayan (SE.5)
Nayan Patel was born in Dombivli, India. He received his Bachelor of Engineering Degree in Instrumentation and Control from Nirma Instititute of Technology, Ahmedabad, India and Master of Science in Engineering degree in Electronic Design Technology from the Indian Institute of Science, Bangalore, India in 2005 and 2007 respectively. For his masters thesis he worked on the performance enhancement of the Tunnel Field Effect Transistor using TCAD simulations. In 2007, he joined Cypress Semiconductors India as a Technology Development engineer. His interests include Emerging semiconductor devices and reliability issues in the submicron technologies.

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Oliver Paul received the Diploma in physics and the D.Sc. degree from the Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, in 1986 and 1990, respectively. Since 1998, he has been a Full Professor with the University of Freiburg, Germany, where he heads the Microsystem Materials Laboratory, Department of Microsystems Engineering (IMTEK). His research interest is in MEMS materials and fabrication technologies, physical microtransducers and microsystems, and microstructures for industrial and life science applications. He is a cofounder of the MEMS company Sensirion AG, a coauthor of over 200 technical articles and four books, and the holder of three patents.

Pazirandeh, Reza (2C.2)
Reza Pazirandeh has diploma in Physics in 1998 from Technical Universtiy of Berlin. He was a scientist at Institut für Halbleiterphysik in Frankfurt/Oder, modeling of SiGe HBTs and LDMOS Transisors and built up of a fully automated load-pull measurement and RF/DC characterization setup (1999-2002). From 2002 - present, he is Scientist at Ferdinand-Braun-Institut für Höchstfrequenztechnik, setup of a reliability lab and responsible for reliability investigation of GaAs HBTs and GaN HEMTs.

Perdu, Philippe (3B.2, 3E.3)
Philippe Perdu is Senior Expert in microelectronics at CNES. He has led the VLSI Failure Analysis CNES laboratory since 1988. He holds an Electronic Specialty MS and Ph.D. and HDR (academic research supervisor). He has authored or co-authored more than 130 papers and 13 patents. He is chairman of CCT MCE, a corporate network on electronic components and MEMS, president (2005 to 2009) of ANADEF, the French FA society and board member of EDFAS (Electron Device Failure Analysis Society) and EUFANET (European Failure Analysis NETwork).

Perng, Dah-Jyh (6C.4)
Dah-Jyh Perng received the M.S. in electrical engineering from National Taiwan Institute of Technology (NTIT, on attaining university status in 1997, name was changed to National Taiwan University of Science and Technology, NTUST) in 1995 and bachelor in electronic engineering from National Taiwan Institute of Technology in 1993. In 1995, he joined TSMC and worked on product reliability assurance (RA) of Q&R. He had joined the tsmc technology qualification and development in N65, N90 and C013. Currently, he is the section manager of failure analysis for tsmc advanced technology and customer.

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Emmanuel Petitprez received the Engineering degree in solid state physics from the Institut National des Sciences Appliquées, Toulouse, France, in 1994, and the Ph.D. degree in materials science from the University of São Paulo, Brazil, in 2001. He was with Serma Technologies, Grenoble, France, as a Characterization Engineer. In 2005 he moved to Freescale Semiconductor, Crolles, France working on interconnect reliability issues in SOI technologies. Since 2007, he has been with the STMicroelectronics Central R&D Laboratory, Crolles, France where he works on the reliability of interconnects for advanced CMOS technology.

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Kin Leong Pey received his Bachelor of Engineering (1989) and Ph.D (1994) in Electrical Engineering from the National University of Singapore. He has held various research positions in the Institute of Microelectronics, Chartered Semiconductor Manufacturing, Agilent Technologies and National University of Singapore. He is currently a Full Professor in the Nanyang Technological University, Singapore, and holds a concurrent Fellowship appointment in the Singapore-MIT Alliance (SMA). He has published more than 140 international refereed publications and 140 technical papers at international meetings/conferences and holds 33 US patents. Dr. Pey is a senior member of IEEE and an IEEE EDS Distinguished Lecturer.

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Jacob CH Phang received both his BA and PhD degrees from the University of Cambridge in 1975 and 1979 respectively. He joined the National University of Singapore in 1979 where he is now Professor at the Centre for Integrated Circuit Failure Analysis and Reliability (CICFAR), Faculty of Engineering. His field of research is in microelectronic device failure analysis and reliability. He is also Executive Chairman of SEMICAPS Corporation, an NUS spin-off company he co-founded in 1988 to commercialize the technologies developed at CICFAR for world-wide distribution.

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Stan Phillips (S'08) received the B.S. degree (with highest honor) in electrical and computer engineering from The Georgia Institute of Technology, Atlanta in 2002, and is currently working toward his M.S. degree at the same university. He is currently involved in the study of the radiation response of semiconductor systems within terrestrial and space-borne applications, with emphasis on SiGe systems. His focus is comprised of the development and application of Radiation Hardening by Design and Radiation Hardening by

Process methodologies for error mitigation in digital and analog architectures.

Pinato, Alessandro (2D.5, 2D.6)
Alessandro Pinato was born in Piove di Sacco (Padova), Italy, in 1982. In 2007 he received the degree (summa cum laude) in Electronics Engineering at the University of Padova, working on the development of an Ion Sensitive Field Effect Transistor (ISFET) based on organic electronics. He is currently working toward the Ph.D. degree in Information Engineering at the University of Padova. His main interests are the characterization and reliability analysis of organic semiconductor devices, in particular OLEDs and organic photovoltaic solar cells (polymeric, molecular and DSC).

Plana, Robert (5E.4, ME.1)
Robert Plana was born on March 1964 In Toulouse. He obtained its PhD in 1993 at LAAS-CNRS and Paul Sabatier University on the Noise modelling and characterization of Advanced Microwave devices (HEMT, PHEMT and HBT) that includes the reliability. In 1993, as associate professor at LAAS-CNRS, he has started a new research area concerning the investigation of millimeterwave capabilities of Silicon based technologies. More precisely, he has focussed on the microwave and millimeterwave properties of SiGe devices and their capabilities for low noise circuits. In 1995, he has started a new project concerning the improvement of the passives on silicon through the use of MEMS technologies. In 1999, he has been involved with SiGe Semi-conductor in Ottawa where he was working on the low power and low noise integrated circuits for RF applications. In the same year, he has received a special award from CNRS for his works on Silicon based technologies for millimeterwave communications. In 2000, he has been professor at Paul Sabatier University and Institut Universitaire de France and he has started a research team at LAAS-CNRS in the field of Micro and Nanosystem for RF and millimeterwave communications. Its main interests are on the technology, design, modelling, test, characterization and reliability of RF MEMS for low noise and high power millimeterwave applications and the development of the MEMS IC concept for smart microsystem. He has built a network of excellence in Europe in this field “AMICOM” regrouping 25 research groups. He has authored and co-authored more than 200 international journals and conferences. In 2004, he has been appointed as Deputy Director of the Information and Communication Department at the CNRS Headquarter. From January 2005 to January 2006, he has been appointed director of the Information and Communication Department at CNRS. He is now heading a research group at LAAS-CNRS in the field of Micro and Nanosystem for wireless communications.

Podgaynaya, Alevtina (4C.6)
Alevtina Podgaynaya received the Dipl.-Ing. degree in Electrical Engineering 2006 from the South-Russian Technical University of Novocherkassk, Russia. The same year she joined Infineon Technologies, where she is currently working on her Ph.D. thesis in close collaboration with the Institute for Solid State Electronics at Vienna University of Technology. Her research field is the improvement of the safe operating area of DMOS transistors.

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Dionyz Pogany received his Dipl.-Ing. degree in solid state engineering from the Slovak Technical University in Bratislava in 1987. In 1994 he received a Ph.D. degree at INSA de Lyon, France. In 1994-95 he was a postdoc at France Telecom, CNET-Grenoble. Since 1995 he is with the Institute of Solid State Electronics, TU Vienna, Austria, where he leads a research team. Since 2003 he is Associate Professor at TU Vienna. His current research interest is in ESD-phenomena, self-heating effects, thermal modeling, current filamentation, breakdown phenomena, power electronics, GaN HEMTs and LEDs, failure analysis, device reliability and development of new optical methods for device characterization. He is author or co-author of more than 170 scientific papers.

Polian, Ilia (E5.3)
Ilia Polian received his Ph. D. degree in Computer Science (with distinction) from the Albert-Ludwigs-University of Freiburg, Germany, in 2003 and diploma (master's) degree in 1999 from the same University. Currently he is a senior member of scientific staff at the Chair of Computer Architecture at the Albert-Ludwigs-University. His previous affiliations were Micronas in Freiburg, IBM Germany R&D in Böblingen and NAIST in Nara, Japan. His research interests include test method and reliability for integrated circuits, MEMS, and nano devices, and security aspects in microelectronic systems.

Pons, Patrick (ME.1)
Patrick Pons received his "Doctorat" in electronics from Paul Sabatier University, Toulouse, France, in 1990. Since 1991 he is a researcher in the CNRS-LAAS (National Scientific Research Center – Laboratory of Analysis and Architecture of Systems) in Toulouse. His research interests are focused in microtechnology and microsensors. In 1995, he started in the lab the study on microtechnology for microwave applications. Now he manages the development of this technology for high frequency Microsystems and develops also pressure sensors for specific applications.

Pop, Eric (4B.5)
Eric Pop joined the Electrical and Computer Engineering (ECE) faculty at the University of Illinois (UIUC) in 2007. His interests are in nanoscale energy transport, power dissipation in nanotube and graphene devices, and novel non-volatile memory. Prior to Illinois, he was with Intel working on phase-change memory and high-k dielectrics for Flash. He also did post-doctoral work at Stanford on the electrical and thermal properties of carbon nanotubes (2005). He received his Ph.D. in EE from Stanford (2005), and holds M.S./B.S. degrees in EE and a B.S. in Physics from MIT (1999). He has been the recipient of the DARPA Young Faculty Award (2008), the Arnold O. Beckman Research Award (2007), the SRC Fellowship, SRC Best Paper and Best Poster awards. He is a member of IEEE, MRS, HKN, and the faculty advisor for the HKN Alpha chapter at the University of Illinois.

Prasad, Chetan (XT.15)
Chetan Prasad received his B.E. from the University of Mumbai (1997) with an emphasis on Electronics and Telecommunications. He then went on to get his M.S. (1999) and Ph.D. (2003) from Arizona State University, where his research was focused on non-equilibrium carrier dynamics and relaxation in III-V semiconductor nanostructures. He joined Intel Corporation in 2003 and is currently a Senior Reliability Engineer with Intel’s Technology Development Quality and Reliability group. His primary responsibilities include research in transistor reliability and dielectric wear-out mechanisms for Intel’s advanced process technologies. He has contributed towards Intel’s 90nm, 65nm and 45nm technologies and is currently working on transistor reliability for the 16nm node. Chetan has authored/co-authored over 30 papers published in peer-reviewed journals and conference proceedings and has 2 patents pending. During his tenure at Intel, he has been the recipient of several awards including the Intel Achievement Award (IAA) and LTD/CQN Divisional Recognition Awards.

Prasad, Krishnamachar (IC.3)
Krishnamachar Prasad received the B.E. degree from Bangalore University, Bangalore, India, the M.Tech. degree from Indian Institute of Technology (IIT), Madras, India, and the Ph.D. degree, all in Electrical engineering, from the University of Western Australia, Nedlands, Western Australia. Since 2007, he has been with the Department of Electrical and Electronic Engineering, Auckland University of Technology (AUT), New Zealand, where he is

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Axel Preusse received his PhD and Master from Dresden University of Technology (Germany) in the field of electrochemistry and physical chemistry. Axel is an AMD Fellow interested in (copper) plating and related metallization processes in high volume manufacturing as well as in research and development.

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Helmut Puchner was born in Steyr, Austria. He received the 'Diplomingenieur' degree in electrical engineering and the PhD degree from the Vienna Technical University in 1992 and 1996,respectively. He joined LSI Logic Corp. in Santa Clara, CA as a device development engineer in 1997. In 2002 he joined Cypress Semiconductor, where he is responsible for transistor developement, TCAD, compact modeling, and device reliability. His research interests include the development of advanced CMOS structures and power transistors including reliability aspects. He has published more than 80 conference/journal articles and hold 16 US patents.

Pufall, Reinhard (PD.1)
Reinhard Pufall received the PhD in physics from the University Bayreuth in 1986. He joined the Siemens Research Centre in 1986. He has worked in different fields as automated design and 2D and 3D full chip simulation for DRAMs in Infineon's business group Memory Products.
He is an expert for interconnect and assembly technologies. He is currently responsible for reliability modelling, accelerated testing and lifetime prediction for automotive power components in the Infineon Automotive business group. He is a founder member of EUCEMAN.

Qin, Jin (4B.1)
Jin Qin received the M. S. and Ph. D degrees in microelectronics reliability engineering from the University of Maryland, College Park, in 2003 and 2007, respectively. His current research topics include NBTI, RTS and circuit reliability simulation and prediction.

Raghavan, Nagarajan (IC.3)
Nagarajan Raghavan received his B.Eng degree in Electronics Engineering from Nanyang Technological University (NTU), Singapore in 2007, S.M degree in Advanced Materials for Micro & Nano Systems from National University of Singapore (NUS) and M.Eng in Materials Science & Engineering from the Massachusetts Institute of Technology (MIT) in 2008. He is currently pursuing his Ph.D. program in the School of Electrical & Electronics Engineering (EEE) at Nanyang Technological University (NTU). He was a recipient of the NTU President's Research Scholarship and the Singapore-MIT Graduate Fellowship in the past. He has been awarded the prestigious IEEE Reliability Society Graduate Scholarship in 2008 in recognition for his achievements in microelectronics reliability. His research interests span a wide range in the field of microelectronics reliability including Gate Oxide Breakdown & High-K dielectric reliability, Copper and Solder Electromigration, Cu-Low-K dielectric breakdown, Through-Silicon Via (TSV) 3D interconnects and wafer bonding. He has authored or coauthored more than 18 papers in peer-reviewed international journals and conferences. He is currently a Student Member of IEEE and the Materials Research Society (MRS).

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Lars-Åke Ragnarsson received a M.S. degree in 1993 and a Ph.D. degree in 1999 in Electrical Engineering from Chalmers University of Technology, Göteborg, Sweden. He did post-doctoral studies at the IBM T.J. Watson Research Center in Yorktown Heights, NY, USA between 2000 and 2002, focusing mainly on electrical characterization of high-k dielectrics. He is since 2002 employed by IMEC in Leuven, Belgium as a senior scientist on high-k dielectrics and metal gates.

Ramaswami, Sesh (2F.5)
Sesh Ramaswami is Sr. Director, Strategy in the Silicon Systems Group at Applied Materials and is currently responsible for driving the Thru-Silicon-Via (TSV) Program. Over the past 14 years at Applied Materials, he has had varied experience in Product Management and Product Development. Prior to Applied, Sesh had thin film process development responsibilities at AMD and at National Semiconductor. A holder of 35 US patents, Sesh has undergraduate and graduate degrees in Chemical Engineering and a MBA.

Ramey, Stephen (XT.15)
Steve Ramey received a B.S. in physics from Carnegie Mellon, an M.S. in electrical engineering from the University of Nevada, and a Ph.D. in electrical engineering from Arizona State University. He started his career with Solid State Measurements, Inc. developing electrical characterization methods for semiconductors. Since 2003, he has been Intel Corporation, where he has contributed to reliability aspects of process development in the 90 nm through 22 nm technology nodes. He has published over 30 journal papers and conference proceedings on high-k dielectrics, electrical characterization, transistor reliability, quantum simulation, and photovoltaic devices.

Rampazzo, Fabiana (CD.4)
Fabiana Rampazzo received the degree in Physics from the University of Padova in 2001 and the Ph.D. degree in electronics and telecommunications engineering in 2005 studying current instabilities, passivation effects and other reliability aspects in AlGaN/GaN HEMTs for Microwave applications. At the moment she is working as laboratory assistant in the same university. Her main research topics includes the electrical characterization of electronic devices grown on wide bandgap semiconductors and reliability studies of the long term stability of microwave devices with particular attention to their failure mode and mechanisms.

Ranjan, Rakesh (BD.3)
Rakesh Ranjan received M.Tech. degree from Indian Institute of Technology Delhi, India and Ph.D. degree in electrical and electronic engineering from Nanyang Technological University, Singapore in 2001 and 2007, respectively. His Ph.D. work involved the high-k/metal gate breakdown analysis. Since 2007, he is working as a Principal engineer in Technology Quality Reliability and Advanced Device Technology divisions of TSMC, Taiwan. He has 22 publications in prestigious journals and prestigious conferences. He is also IEEE member since 2003.

Rao, Rahul (CR.2)
Rahul M. Rao received the B.E degree in electronics engineering from the University of Bombay (Mumbai) in 2000, and the M.S. and PhD degrees in electrical engineering from the University of Michigan, Ann Arbor in 2002 and 2004 respectively. He is currently a Research Staff Member at IBM's T.J. Watson Research Center, Yorktown Heights, NY. His research interests include low-power, adaptive circuits, device degradation and life-time issues in high-performance VLSI designs.

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Dr. V. Ramgopal Rao is a Professor in the Department of Electrical Engineering, IIT Bombay. Dr. Rao has over 200 publications in the area of Electron Devices & Nanoelectronics in refereed international journals and conference proceedings. Prof. Rao received the coveted Shanti Swarup Bhatnagar Prize in Engineering Sciences in 2005 awarded by the Hon'ble Prime Minister, Govt of India for his work on Electron Devices. Dr. Rao is an Editor for the IEEE Transactions on Electron Devices in the CMOS Devices and Technology area and serves on the program committees of various international conferences including the IEDM. Dr. Rao is a Fellow of the Indian National Academy of Engineering and a Fellow of the Indian Academy of Sciences.

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Meredith L. Reed received the B.S. and Ph.D. degrees in material science and engineering from North Carolina State University, Raleigh, North Carolina in 1997 and 2003, respectively. She has been with the US Army Research Laboratory, Maryland since 2006. Her current research focuses on the development of III-Nitride optoelectronics devices and their transition to emitter and sensing technologies. She has contributed over 30 conference and journal publications in the area of III-Nitrides which have been cited more than 500 times in the literature.

Reisinger, Hans (XT.6)
Hans Reisinger received his diploma in physics (1979) and his Ph.D. (1983) both from the Technical University of Munich. In 1986 he joined the Siemens Semiconductor Department (now Infineon). His work was focused mostly on the study of thin dielectrics and interfaces in DRAMs and NVMs. Currently he is with the Reliability Methodology group and works on MOSFET degradation.

Robins, Scott (3B.1)
Scott Robins is currently Vice President of Technology at T-RAM Semiconductor. He has developed several generations of bipolar, CMOS, E2CMOS, BiCMOS, BiFAMOS, and T-RAM technologies, in both engineering and management roles. He received the B.S. (1984) and M.S. (1984) in Electrical Engineering from the Massachusetts Institute of Technology.

Rodríguez, Rosana (XT.16)
Rosana Rodríguez received the Ph. D. in Electrical Engineering from the Universitat Autònoma de Barcelona in 2000. Funded by the Fulbright program, she worked on devices and circuits reliability at the IBM Thomas J. Watson Research Center (USA). Currently, she is an associate professor at the Universitat Autònoma de Barcelona. Her research interests are focused on the effect of CMOS dielectric failure on the performance of devices and digital and analogical circuits. She analyses, experimental and theoretically, different failure mechanisms such as dielectric degradation and breakdown, NBTI and Channel Hot Carriers on state-of-the-art gate dielectrics under DC and AC conditions.

Roig, Jaume (4C.2)
Jaume Roig was born in Roses, Catalonia, Spain, in 1976. He received the B.S. degree in physics and the Ph.D. degree in microelectronics engineering from the Universitat Autonoma (Barcelona, Spain) in 1999 and 2004, respectively. From 2000 to 2005, he was with the CNM-IMB/CSIC, Barcelona. He joined LAAS/CNRS (Toulouse, France) in 2005 to continue his research on advanced power devices. Finally, he moved to ON-Semiconductor (Oudenaarde, Belgium) in 2006, where he is currently working on design and development of discrete and integrated semiconductor devices. He has authored and coauthored about 80 scientific articles in international journals and conferences.

Rothleitner, Hubert (5F.1)
Hubert Rothleitner graduated as a „Diplom Ingenieur“ in electrical engineering at the Technical University of Graz, Austria in 1982. From 1982 till 1985 he has been working as an engineer for automation systems with Siemens AG Erlangen and Karlsruhe. In 1985 he joined Infineon (former Siemens Semiconductors) Villach, Austria, where he was involved in designing power supply chips for telecommunication applications. Contributing to the up growing smart power technology development (SPT) he worked on HS- and LS-switches as well as designs for safety applications e.g. airbag or breaking systems for the automotive industry. As a Senior Principal for smart power design at Infineon his fields of interest are novel system architectures with new technologies and device concepts combined with reliability related aspects for integrated smart power devices, especially MOS-surface- and bipolar- parasitics, latch-up immunity and ESD-protection.

Roussel, Philippe J. (2B.5, 5C.2, XT.13)
Philippe J. Roussel received the diploma in Electrical Engineering from the Industriële Hogeschool of Ghent, Belgium, in 1983. His first job with SIEMENS AG at the Oostkamp site involved IEEE controlled instrumentation. In 1984, he joined the ESAT laboratory of the Katholieke Universiteit Leuven, Belgium as an assistant in a reliability research project on plastic encapsulation, where he developed several programs for the analysis of test failure data. From 1987, he assisted in a government funded project on electromigration in the Analysis and Reliability Group of the Materials and Packaging division of the Interuniversity Micro-Electronics Center (IMEC), Leuven, Belgium, which also resulted in a maximum likelihood fitting program for the assessment of statistical distributions and acceleration models from reliability data. From 1991 till 2000, he worked on analysis techniques like microprobe, TEM and Spectroscopic Ellipsometry in the PT/MCA group, while continuing his research on Reliability Statistics, Statistical Process Control and Data Analyis in the PT/DREM group. At present he also works in a multidisciplinary team on the statistics required for Technology Aware Design. He co-authored papers in fields as diverse as handheld calculator programming, virology, Spectroscopic Ellipsometry, ESD, oxide and interconnect reliability, and Technology Aware Design.

Roux, Julien-Marc (5D.4)
Julien-Marc Roux received the M.S.E.E. degree from Joseph Fournier University, Grenoble, France, in 2001 and from the Polytechnic Institute of Grenoble (INPG). Afterwards, he went to work for Dolphin delegation, Meylan, France, in the Design for Test team. In 2004 he joined STMicroelectronics, Crolles, France, where he works on the HCI reliability in the Electrical Characterization and Reliability Team.

Ruan, Jinyu (5E.4)
Jinyhu Ruan was born in Guang Dong, China and grew up in French Guiana, where he received his Bachelor’s degree in Electronics, Electrical Engineering and Automation. He received the Master of Science degree in Electrical Engineering for High Frequency Telecommunication Systems from the University of Marne la Vallée, Paris, France in 2006. He is currently working toward the Ph.D. degree at the Laboratoire d'Architecture et d'Analyse des Systèmes at the Centre National de la Recherche Scientifique (LAAS-CNRS), France. His Ph.D. studies involve in reliability of RF MEMS, from design modeling to testing. His main field of interest is in the electrical characterization of RF MEMS, particularly the dielectric charging effects and electro-static discharges failures.

Ruther, Patrick (E5.3)
Patrick Ruther studied physics and received his PhD from the Technical University Karlsruhe in 1996 with his work on a miniaturized bending test system using the LIGA process. Since 1998 he is groupleader at the Department of Microsystems Engineering,

University of Freiburg and responsible for projects on piezoresistive stress sensors, i.e. tactile force sensor for metrology of microcomponents, and respective sensor characterization as well as on intracortical neural probes. Since 2006 he is Technology Coordinator of the EU-founded project NeuroProbes.

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Jason T. Ryan (S'04) received the B.S. degree in Physics from Millersville University, Millersville, PA in 2004 and the M.S. degree in Engineering Science from The Pennsylvania State University, University Park, PA in 2006. He is currently working towards a Ph.D. in Materials Science and Engineering at The Pennsylvania State University. His current research involves the atomic-scale mechanisms involved in NBTI. He currently serves on the management committees of the International Integrated Reliability Workshop and the International Reliability Physics Symposium.

Sachelarie, Dan (CD.3)
Dan Sachelarie, professor of Semiconductor Devices at University Valahia, Targoviste, Romania. 1971: diploma in Electronics Engineering. 1983: Ph.D. in Physics. 1971 – 1997: senior research scientist at Institute for Electronic Components (IMT), Bucharest. 1992 – 1993: postdoctoral fellow, CNRS, Paris, France. 1997 – 1998: member of Romanian Government, state counsellor to the Prime Minister. 1998 – 2000: counsellor to the president of Romanian Chamber of Deputies. 1998 – 2002: member of Administration Board of Romanian Television Company. 1997 – 2001: president of Romanian Scientific Forum (FORS). 2001 – 2009: professor.

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Hyun Chul Sagong received the B.S. (2008) in electronics engineering from the Pusan National University (PNU), Pusan, Korea. He is currently in M.S. and Ph.D. integrative program cource at the Pohang University of Science and Technology (POSTECH), Pohang, Korea. His main research interests include CMOS devices and RF measurement.

Saha, Prabir (2C.4)
Prabir K. Saha (S'05) received his B.Tech degree in instrumentation engineering and his M.S. degree in electrical engineering from the Indian Institute of Technology, Kharagpur, WB, India, in 2004 and 2006 respectively. He is currently a PhD student in the department of electrical and computer engineering at Georgia Institute of Technology. His research interests include design of RF and millimeter-wave integrated circuits, wireless communication, data converters and solid-state semiconductor devices.

Sahhaf, Sahar (5C.2)
Sahar Sahhaf received the M.Sc. degree in electrical engineering from the Catholic University of Leuven, Belgium, in 2006. Currently, she is working toward the Ph.D. degree at the KULeuven university (Belguim) and IMEC. The main focus of her work is on the reliability of high-κ gate dielectrics and metal gates.

Saitoh, Masumi (2A.3)
Masumi Saitoh was born in Yokohama, Japan, in 1978. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2000, 2002, and 2005, respectively. In 2005, he joined the Advanced LSI Technology Laboratory, the Research and Development Center, Toshiba Corporation, Yokohama, Japan. He has been engaged in the research on the carrier transport properties in nano-scaled MOSFETs.

Sakamoto, Toshitsugu (4B.3)
Toshitsugu Sakamoto received the B.S. (1989), M.S. (1991) and Ph.D. in electrical engineering from Osaka Univ. After joining NEC Corp., Japan, in 1991, he worked on nanometer-scale devices as hot electron transistors, single electron devices, and is recently working on the solid-electrolyte devices in Device Platforms Res. Labs. of NEC Corp. From 1999 to 2000 he was also a visiting researcher in California Institute of Technology, Pasadena, CA.

Salcedo, Javier (EL.5)
Javier A. Salcedo received the B.S in Electronic Engineering from Universidad Simón Bolívar (USB), and M.S. and Ph.D. degree in Electrical Engineering from University of Central Florida (UCF). He has been a researcher at the USB Solid-State Electronics Lab; a visiting scholar at Intersil Corporation; and a guest researcher at the National Institute of Standards and Technology. He is currently with Analog Devices. Dr. Salcedo is a member of the IEEE, the AAAS, and the ESDA. He is an active contributor in the area of electron devices and electrostatic discharge applications and regular invited referee in per-review technical journals.

Salling, Craig (3B.1)
Craig Salling is currently responsible for product and technology reliability at T-RAM Semiconductor, where he has worked since 2002. Prior to this, Dr. Salling has developed and implemented on-chip ESD protection, characterized Flash cell reliability, assessed and ensured EPROM product reliability, established accurate sub-20ps e-beam timing measurements, demonstrated reproducible atomic-scale patterning of silicon surfaces, investigated atomic-scale mechanisms of film growth, and measured the switching field of individual sub-micron single-domain magnetic structures. He holds 34 patents and has published over 25 technical papers. He received a Ph.D. in Physics in 1990 from the University of California at San Diego.

Salman, Akram A. (5F.4)
Akram Salman received his B.S. degree in electrical engineering from Alexandria University, Egypt, 1996, the M.S. degree from Arab Academy for Science and Technology, Egypt, 1999 and the Ph.D. degree from George Mason University, Fairfax, VA, (2002) in electrical engineering. His Ph.D. research was in the area of electrostatic discharge (ESD) and hot carrier reliability (and their interdependence) for deep sub-micron bulk and SOI CMOS technologies. During the summers of 2000 and 2001 he worked at IBM Microelectronics Division on a student internship. He joined the Technology and Reliability Engineering department at Advanced Micro Devices (AMD) in 2002. In 2008, he joined the Analog Technology Development group at Texas Instruments (TI) working on the ESD development for various analog technologies.

Samukawa, Seiji (4A.6)
Dr. Seiji Samukawa was born on April 1, 1959. He received B.S. degree from Keio University in 1981 and Ph.D in 1992, respectively. Now, he is Professor of Institute of Fluid Science, Tohoku University and worked on the fundamental research of plasma etching, plasma CVD, beam technologies and bio- nanoprocess for ULSI and future nano-scale devices.

Sanchez, Kevin (3B.2, 3E.3)
Kevin Sanchez received the M.S. in microelectronics from the Joseph Fourier University of Grenoble in France in 2003. He joined the French Space Agency (CNES) in partnership with Credence DCG in 2003 to perform a Ph. D in the field of IC failure analysis and defect localization through laser stimulation techniques. He joined CNES in 2006. He is especially involved in failure analysis and expertise of ICs.

Sato, Motoyuki (2B.3, 3E.5, XT.4)
Motoyuki Sato received the B.S. and M.S. degrees in physical engineering from the University of Tokyo, Tokyo, Japan, in 1996 and 1998, respectively, and the Ph.D. degree in engineering from University of Tsukuba in 2008. He joined Toshiba Corporation, Yokohama, Japan in 1998, and has been engaged in the research for semiconductor device process. He joined the Semiconductor Leading Edge Technologies Inc. (Selete) since 2006. He received the best paper award in IWDTF 2008. His current interests and activities

include the study of the degradation physics in high-k gate dielectrics. Dr. Sato is a member of technical committee in IRPS 2009.

Schlunder, Christian (XT.6)
Christian Schlünder has received his Dipl.-Ing. (1999) in electrical engineering and his doctoral degree in engineering science (2006) accompanying his regular work (both from the University of Dortmund, Germany). From 1998-1999 he worked in a cooperative program between Siemens Corporate Research Labs in Munich and the University of Dortmund 1999 he joined Infineon as a member of the Corporate Research Department, where he was active in research on hot carrier stress in mixed signal applications. Since 2000 he works in the Corporate Reliability Methodology Group. There he manages process qualification projects for various state-of-the-art CMOS-Technologies and evaluates the reliability of innovative technologies like Hi-k, Metal-Gates, SOI, Strained Silicon, etc. Furthermore he leads the NBTI-research for Infineon. His current work is focused on recovery phenomena. Christian Schlünder has published several papers in various conference proceedings and microelectronic journals. Additionally, he has presented invited talks and tutorials at many conferences such as 'IRPS' or 'ESSDERC'. He is frequently a member of the Technical Program Committee of the IEEE-conferences 'IRPS', 'IRW' and referee of several IEEE journals. Moreover he is involved in JEDEC standards developments.

Schneider, Jens (6C.3, EL.2)
Jens Schneider received his diploma in physics (Dipl. Phys.) in 1995 from the University of Kaiserlautern working on the condensation of quasi-particles in field theories. He then moved to Munich where he he received his Ph.D. from Ludwig-Maximilians-University in 2001 in the field of atom lasers and Bose-Einstein condensation. Since then he is working with Infineon Technologies, first in the field of modelling of process effects in photomask lithography. Since 2003 he is working in the Infineon ESD/LU group where is involved with process and device simulation of ESD phenomena and with the development of HV CMOS ESD protection concepts.

Schram, Tom (4A.5, XT.13)
Tom Schram received a degree in chemical engineering in 1994 and a Ph.D in engineering in 1999 from the Vrije Universiteit Brussel, Belgium. Since 2000 he is working at IMEC as senior scientist with special focus on high-k and metal gate integration.

Schrimpf, Ronald (2G.3)
Ron Schrimpf received BEE, MSEE, and PhD degrees from the University of Minnesota and he has been a professor at the University of Arizona and Vanderbilt University. He is the Orrin Henry Ingram Distinguished Professor of Engineering and Director of Vanderbilt's Institute for Space and Defense Electronics. Ron has served as General Chairman of the IEEE Nuclear and Space Radiation Effects Conference and Chairman of the IEEE Radiation Effects Steering Group.

Schwaha, Philipp (5D.2)
Philipp Schwaha was born in Vienna, Austria, in 1977. He studied electrical engineering at the Technische Universität Wien, where he received the degree of Diplomingenieur in 2004. He joined the Institute for Microelectronics in June 2004, where he is currently working on his doctoral degree. His research activities include circuit and device simulation, device modeling, and software development.

Scipioni, Larry (3E.2)
Larry Scipioni received his Ph.D. in physics in 1996, doing studies on properties of ultrathin films. He has worked in charged particles optics development his entire career. He worked first as an ion source and optics scientist at the Micrion Corporation (later FEI Company), and has held various project and functional management roles in research and development. He is currently with Carl Zeiss SMT in Massachusetts, serving as Director of Applications Research for the Orion helium ion microscope.

See, K.S. (XT.14)
K.S. See received the B.Eng. (Hons.) degree and Ph.D. from the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. Currently, he is working in Chartered Semiconductor.

Seguineau, Cedric (ME.1)
Cédric Seguineau (born in Bordeaux, France in 1983) received his french engineer degree "Ingénieur de l'Ecole Centrale de Lyon" in 2005. In parallel, he has obtained his MSc degree in material and multimaterial engineering from the University of Lyon. Since November 2005, he is working as a PhD student on mechanical characterization of layered materials for MEMS applications. His PhD is made in collaboration between NovaMEMS, which provides unique services in technology analysis and qualification of micro technologies, and the INP (Institut National Polytechnique) of Grenoble. Most of his experiments are leading at the laboratory AQ/LE in the CNES, Toulouse.

Segura, Jaume (EX.3)
Jaume Segura received the M.S. and Ph.D. degrees from the Balearic Island University and the Polytechnic University of Catatonia in Spain respectively. He is currently a Full Professor of the Physical Department at the Balearic Islands University (UIB) in Palma de Mallorca, Spain. He was on leave from UIB in 1994 and 2001 as invited researcher at Philips Semiconductors, USA, and Intel Corporation respectively. His research interests include device and circuit modeling, VLSI design and test, advanced compact modeling, defect and, fault modeling, development of parametric test methods for nanometer technologies, and low-temperature design techniques.

Seifert, Norbert (2H.3)
Norbert Seifert received Diplom Ingenieur and Ph.D. degrees in physics from the Technical University of Vienna, Vienna, Austria, in 1990 and 1993, respectively. He also holds an M.S. degree in physics from Vanderbilt University (Nashville, TN, May 1994). Dr. Seifert is currently the radiation effects lead in Intel Corporation. Prior to joining Intel in 2003, he worked in the fields of compact modeling, device reliability and digital design in the Alpha Development Group (DEC, CPQ, HP).

Sekiguchi, Takashi (3E.5)
Takashi Sekiguchi received the B. S. degree in physics from Kyoto University in 1981, and the M. S. and Ph. D. degrees in physics from Tohoku University in 1983 and 1995. He has been engaged in the study of defects in semiconductors, especially characterization of electrical and optical properties of individual defects by electron beam techniques such as cathodoluminescence and electron-beam-induced current (EBIC). With these techniques, he has clarified the electrical/optical properties of dislocations in Si. Then, he has extended his research for the study of quantum dots, semiconductor nanostructures, and novel MOSFET etc. His quantitative CL/EBIC system was effective to directly image the weak points in high-k MOSFETs.

Sekine, Katsuyuki (4A.2)
Katsuyuki Sekine, received the B.S. (1995), M.S. (1997), and the Ph.D. (2000) in electronic engineering from Tohoku University, Sendai, Japan. He is currently engaged in advanced gate dielectric film-formation process in the Process and Manufacturing Engineering Center, Toshiba Corp., Semiconductor Company, Yokohama, Japan.

Serov, Andrey (MY.3)
A. Serov was born in Russia, in 1982. He received the M.S. degree in physics from St-Petersburg State Polytechnical University, Russia

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Shaviv, Roey (IC.12)
Roey Shaviv received his Ph.D. in chemistry in 1988 from the University of Michigan, in Ann Arbor. He is a senior integration and applications technologist at Novellus Systems Inc. He joined Novellus in 2001 and is specializing in reliability and integration issues associated with copper / low k interconnects. Prior it this, he was the Etch Engineering Section Head, and earlier the Thin Films and CMP Engineering Section Head, at Tower Semiconductors. He was a Lecturer at the Chemistry Department of the University of Michigan and a Research Associate in the Chemistry Department of University of Illinois, Chicago.

Shaw, Thomas (6A.1, IC.10)
Thomas M. Shaw is a Research Staff Member at the IBM Thomas J. Watson Research Center. He joined the physical sciences department at IBM Research in 1984 and currently has a position in the silicon technology department. Dr. Shaw received his Ph.D. in materials science from the University of California at Berkeley in 1981. Prior to joining IBM Dr. Shaw was a member of the technical staff at Rockwell International's science center and a postdoctoral associate at Cornell University. He is a fellow of the American Ceramics Society and has authored or co-authored more that 200 publications and 30 patents.

Sheng, Kuang (4B.1)
Kuang Sheng received the B.Sc. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 1995, and the Ph.D. degree in electrical engineering from Heriot–Watt University, Edinburgh, U.K., in 1999. He was a Researcher with the Cambridge University, Cambridge, U.K., for three years and is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Rutgers University, Piscataway, NJ, USA. His research areas include various aspects of power semiconductor devices and ICs on SiC, Si, and SOI. He has authored or coauthored around 80 technical papers in international journals and conferences, and he is the holder of a patent.

Sheng, Lieyi (FA.4)
Lieyi Sheng received the Ph.D. in electrical and electronic engineering from the Univ. of Brussels, Belgium. He is a principle engineer at ON Semiconductor, working on technology reliability qualification. He has authored or co-authored more than 20 publications in semiconductor, MEMS, and optoelectronics.

Shigematsu, Hisao (2C.1)
Hisao Shigematsu received the B.E. degree from Osaka University, Osaka, Japan, in 1990, and Ph.D. degree from Osaka University, in 2007. He is currently a Senior Researcher of the Advanced Device Laboratory, Fujitsu Laboratories Ltd., Atsugi, Japan. In 1990, he joined the Fujitsu Laboratories, Kanagawa, Japan, where he has been engaged in research on development of high-speed compound semiconductor devices (HEMTs, HBTs) and integrated circuits for fiber-optic communication systems. In 2003, he was a Visiting Researcher with the University California at Santa Barbara, where he was involved with millimeter-wave CMOS circuits. His current research interests include GaN devices and circuits for high power applications. Dr. Shigematsu is a member of Institute of Electrical and Electronic Engineers.

Shih, Jiaw-Ren (6C.4, BD.3, IC.13)
J.R. Shih is the Academician in TSMC Academy, and also serves as the mainstream technology quality and reliability department manager at TSMC. Prior to joining reliability division in 2000, he served as the transistor designer at device department of R&D since 1992. Currently, he focused on the logic front-end process qualification, memory IP reliability qualification and the study of advanced device reliability physics. Dr. Shih served on the IRPS Technical Committee in 2002, 2004 ~ 2009 for Transistor, Process Integration and Dielectric Sections, respectively. He holds 48 U.S. patents and 40 Taiwan patents, and also published more than 41 technical papers.

Shih, Wei-Kai (NA.1)
Wei-Kai Shih Received Ph.D. in electrical engineering from University of Texas at Austin in 1997, with a focus on device physics. He joined Intel in 1997 and has since worked on many modeling projects in the area of thermal, device reliability, gate leakage, analog-RF, and interconnect. He currently leads a group of 15 CAD developers to develop interconnect, process variation, and reliability models and simulation tools, including application of CAD tools to guide technology targeting. He has authored 25 journal and conference papers in the area of device simulation or compact modeling.

Shih, Yen-Hao (3C.5)
Yen-Hao Shih received the B.S.E.E. degree from National Taiwan University in 1997, and the Ph.D. degree in electrical engineering from National Taiwan University in 2002. He joined Emerging Central Lab, Macronix in 2002, working in the area of SONOS Flash nonvolatile memory and Phase Change Memory. His research includes device engineering, process development, as well as nonvolatile memory reliability.

Shimizu, Tatsuo (4B.2)
Tatsuo Shimizu received the B.S.(2002) and M.S.(2006) in apllied physics from Waseda University, Tokyo, Japan. In 2006, he joined NEC Electronics Corp., Kawasaki, Japan. He has been engaged in hot carrier and NBTI reliability in MOS devices.

Shimokawa, Junji (XT.4)
Junji Shimokawa received the B.S. degree in mathematical engineering from Osaka Prefecture University, Osaka, Japan, in 2003 and the M.S. degree in information science and technology from Osaka University, Osaka, Japan, in 2005. He joined Toshiba Corporation, Yokohama, Japan in 2005, and has been engaged in the development of TCAD system for efficient development of the semiconductor device. He concurrently joined the Semiconductor Leading Edge Technologies Inc. (Selete) since 2007. His current interests and activities include the implementation of the function for reliability simulation to 3D TCAD system HyENEXSS.

Shinohara, Mamoru (6C.2)
Mamoru Shinohara received the B.S. degree in applied physics from Waseda University, Tokyo, Japan, in 1981. From 1981 to 1989, he was with Oki Electric Industry Co. Ltd., Tokyo, Japan. In 1989, he joined Sony Corporation, Tokyo, Japan, where he has been involved in developing various silicon processes and devices, including BiCMOS, high-voltage devices, ink-jet printer heads, field emission devices, finger-print sensors, and ESD protection devices. Mr. Shinohara is a member of the Japan Society of Applied Physics, the Institute of Electrical Engineers of Japan, the Institute of Electronics, Information and Communication Engineers, and the Japan Institute of Electronics Packaging.

Shinosky, Mike (5B.1)
Mike Shinosky received an Associate of Engineering degree in Electronic Engineering from A.T.E.S. Technical Institute of Niles, Ohio in 1982. Mike joined IBM in 1982, where he was responsible for building and running Soft Error Rate testers for DRAM Memory products. In 1985 he began T2 Functionality Qualification testing of DRAM memory cards for large scale server applications. In 1999 Mike transferred to an ASICS department doing book level Physical Design Mask Layout work. In 2003 Mike joined Technology Reliability Engineering, where he is currently and primarily responsible for TDDB testing of BEOL Dielectric technologies.

Shiraishi, Kenji (2H.4)
Ken Shiraishi received the B.S. (1978) in engineering from Osaka University, Japan. He joined Sony Corp. in 1988. He is a member of the Memory Department, LSI Business Division, Semiconductor Business Group. His interests are cosmic ray-induced soft error in LSI, reliability engineering in SRAM devices.

Shrivastava, Mayank (6C.3, EL.2)
Mayank Shrivastava was born in Lucknow, Uttar Pradesh, India, in 1984. He received the B.S. degree in engineering from Rajiv Gandhi Technical University, Bhopal, India, in 2006. In July 2006, he joined the Indian Institute of Technology (IIT) Bombay, Mumbai, India, where he has been working toward the Ph.D. degree in the Center for Nano Electronics, Department of Electrical Engineering, as a Research Scholar from Jan 2008. He was working as a Visiting Research Scholar with Infineon Technology AG, Munich, Germany from April 2008 to Oct 2008. He was also a co-recipient of Intel's AAF-2008 best research paper award in circuit design category. His current research interests include device and circuit co-optimization for ESD and I/O applications, hot carrier and NBTI reliability, novel devices and its circuit applications, FinFETs, tunnel FETs, Flash memories, nonvolatile analog memories, and neural processing. He has 5 US and 1 Indian patent pending in the fields of ESD, I/O devices, FinFETs, and nonvolatile analog memory.

Shuler, Robert (2G.3)
Robert Shuler works for NASA's Johnson Space Center, developing and evaluating RHBD techniques for over ten years. He holds 5 patents, including a multi-channel instrumentation chip architecture, a practical active-capacitor filter, hardware support for artificial intelligence, and the TAG or Guard Gate. He received a BSEE degree from Mississippi State University in 1972, and an MSEE from Rice University in 1974. Other interests include the sociology of reliable systems, FPGA architectures to support high level languages, and gravitomagnetic effects at cosmological scales. Mr. Shuler has received the NASA Exceptional Achievement Medal, and Director's Innovation Award.

Sienkiewicz, Magdalena (3E.3)
Magdalena Sienkiewicz received the M.S. degree in Telecommunications and Electrical Engineering from the University of Technology in Gdansk (Poland) and ENST Bretagne in Brest (France) in 2006. Since 2006 she is a Ph.D. student at the University of Bordeaux. Her research, on dynamic laser stimulation techniques for analog and mixed mode ICs, is implement at CNES & Freescale Semiconductor labs in Toulouse.

Sijbrandij, Sybren (3E.2)
Sybren Sijbrandij has focused on the development of scientific instrumentation during his pursuit of degrees in Applied Physics (University of Groningen) and Materials Science (University of Oxford), and during his subsequent career at Oak Ridge National Laboratory, FEI Company and Carl Zeiss SMT. Areas of expertise include 3D atom-probe field-ion microscopy and focused ion beam processing and microscopy. In his current role as a scientist and program manager at Carl Zeiss SMT, he works on advancing the capabilities of the helium ion microscope.

Simoen, Eddy (2B.5)
Eddy Simoen obtained his Masters in Physics Engineering ('80) and Doctoral Degree in Engineering ('85) from the University of Gent (Belgium). His doctoral thesis was devoted to the study of trap levels in high-purity germanium by deep-level transient spectroscopy. In 1986, he joined IMEC to work in the field of low temperature electronics. His current interests cover the field of device physics and defect engineering in general, with particular emphasis on the study of low-frequency noise, low-temperature behavior and of radiation defects in semiconductor components and materials. He is an IMEC Scientist, currently involved in the study of defect and strain engineering in high-mobility and epitaxial substrates and defect studies in germanium. In these fields, he has (co-) authored over 900 Journal and Conference papers and in addition 11 book chapters and a monograph on Radiation Effects in Advanced Semiconductor Devices and Materials (Springer, 2002) whereof the Chinese translation has been published in March 2008. He was also a co-editor of the book on Germanium-based Technologies - from Materials to Devices (Elsevier March 2007). A new book on the "Fundamental and Technological Aspects of Extended Defects in Germanium" will be published by Springer in January 2009. He acted as co-editor of four International Conference Proceedings and was a lecturer at the International Noise School held at IMEC in 1993, at the ENDEASD Workshop in Santorini (Greece; april 1999) and Stockholm (Sweden, June 2000) and at the EUROSOI Workshop in Leuven (January, 2007).

Singh, Kaushal (3C.6)
Kaushal K Singh is a senior member of technical staff at Applied Materials, Santa Clara, CA, USA.

Singh, Pawan (3C.6)
Pawan K Singh received B. Tech. and M. Tech. combined degrees (2006) from Electrical Engineering department of the Indian Institute of Technology (IIT) Bombay, India. Since 2006, he is pursuing Ph.D. in Electrical Engineering department in IIT Bombay. He is an AMAT fellow for PhD in IIT Bombay since 2006. He has been a graduate intern at Applied Materials, Santa Clara, CA from June 2007 - July 2008. His research interests include technology development, physics, and reliability characterization of non-volatile memories. He is currently working on metal nanocrystal based non-volatile memories for NAND application. He is a student member of the IEEE.

Song, Min-Woo (XT.3)
Min-Woo Song received Ph.D. degree in chemical engineering from Yonsei university in Seoul, Korea in 2003. He has been a senior engineer position at Samsung Electronics in process development team of MIM Capacitor and high-k gate dielectric/metal gate module.

Song, Peilin (6B.3)
Peilin Song received the Ph.D. degree in electrical engineering from the University of Rhode Island. He is with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, where he is a Manager of the Circuit Diagnostics and Test Technology Department. He joined IBM in 1997 and has since worked in the area of design for testability, fault diagnostics, fault modeling, circuit simulation, and laser stimulation technique. He has more than 50 publications, holds 21 U.S. patents with several patents pending. Dr. Song won the IEEE Electron Device Society Paul Rapparport Award, in 2004.

Song, Seung-Hyun (PI.1, XT.8)
Seung-Hyun Song received the B.S. (2004) in electronics engineering from the Pohang University of Science and Technology (POSTECH), Pohang, Korea. He is currently in M.S. and Ph.D. integrative program course at POSTECH. His main research is related to CMOS devices.

Spinelli, Alessandro S. (3C.1)
Alessandro S. Spinelli was born in Bergamo, Italy in 1966. He received the Laurea (cum laude) and Ph.D. degrees in electronics engineering from the Politecnico di Milano, Milano, Italy. In 1995 he was a Visiting Scholar with the University of Tennessee Space Institute, Tullahoma, TN, where he worked on single-molecule detection in solution, and in 1996 he worked as a consultant with the Central Department of Research and Development, STMicroelectronics, Agrate Brianza, Italy. In 1997 he became Assistant Professor with the Politecnico di Milano and was with the Università degli Studi dell'Insubria, Como, Italy as an Associate Professor of electronics in 1998. In 2001 he was a Visiting Professor

at the Institute National Polytechnique de Grenoble, Grenoble, France. He is currently a Full Professor of electronics with the Politecnico di Milano. He has conducted experimental and theoretical research in electronics instrumentation and microelectronics, co-authoring more than 100 papers published in international journals or presented at international conferences, and serving in the technical committees of the IEDM and IRPS conferences. His current research interests include experimental characterization and modeling of non-volatile memory cells reliability, development of innovative non-volatile memories, modeling and simulation of nanoscale MOS devices and circuit development for biological signal readout.

Stathis, James (5D.1, CR.2)
Jim Stathis received the bachelor's in physics from Washington University in St. Louis (1980), and the Ph.D. in physics from the Massachusetts Institute of Technology (1986), joining the IBM Research Division the same year. At IBM the focus of his work has been the electrical properties of point defects in SiO2, including basic studies of defect structure using magnetic resonance and electrical measurement techniques, and the role of defects in wearout and breakdown. He is the author or coauthor of more than 100 research papers and over 60 invited talks. From November 2005 to February 2007 he served as Technical Assistant to the Vice President for Science and Technology, IBM Research Division. In February 2007 he became manager of High-k/Metal-Gate Characterization and Reliability, IBM Research. Jim has served on technical program committees for SISC, INFOS, IRPS, ESREF, IPFA, and other conferences, served as Chair of the dielectrics sub-committee for the 2003 IRPS in Dallas, and is on the IRPS management committee. He is the Technical Program Chair for IRPS 2009. He has presented tutorials on CMOS reliability at IRPS, ESREF, and IPFA and is an Associate Editor of the journal Microelectronics Reliability. He is a Senior Member of IEEE and a Fellow of the American Physical Society.

Stecher, Matthias (4C.6)
Matthias Stecher studied Electrical and Electronic Engineering at the VaTech (USA) and at the Rheinisch-Westfälische Technische Hochschule Aachen (Germany) where he received his PhD in 1995. Between 1989 and 1994 he was involved in the development of device and circuit simulation tools. He joined Infineon Technologies in 1994 and has been project manager for several Smart Power Technologies of Infineon. Since 2003 he has been involved in the thermo-mechanical optimization of chip-package systems. Currently, he holds the position of a technical advisor in the fields of power technology and package development. He holds more than 20 patents.

Stellari, Franco (6B.3)
Franco Stellari received M.S. and Ph.D. degrees in electronics engineering from the Politecnico di Milano, Italy, in 1998 and 2002 respectively. He subsequently joined IBM Watson Research Center as a PostDoc becoming a Research Staff Member in 2004. His major interests are the development and use of new optical methodologies for testing VLSI circuits. He has more than 50 international publications, 6 granted patents and several more pending. He has won the IEEE EDS Paul Rappaport Award for the best Trans. on Electron Devices of 2004, and two Best Paper Awards at the ESREF conference in 2002 and 2004.

Stimpfl, Franz (5D.2)
Franz Stimpfl was born in Vienna, Austria, in 1980. He studied computer science at the /Technische Universität Wien/, where he received the degree of /Diplomingenieur/ in 2007. He joined the Institute for Microelectronics in October 2007, where he is currently working on his doctoral degree. His research activities include mesh generation and modern software paradigms.

Strijbos, Remco (5E.2)
R.C. (Remco) Strijbos received the M.S. degree in experimental physics from the University of Leiden in 1991, and the Ph.D.degree from Delft University of Technology in 1997. He conducted post-doctoral research on mode-locked terahertz p-Ge lasers at the University of Central Florida, Orlando, and on polarization control of VCSELs at Eindhoven University of Technology. In 2001, he joined JDS Uniphase, Eindhoven, working on (widely) tunable semiconductor lasers. In 2005, he joined Philips Semiconductors (now NXP), Nijmegen, to develop BAW filters. In 2008, he joined the base station group at NXP to develop advanced LDMOS transistor technology.

Su, David (6C.4, IC.13)
David Su is currently Director of Failure Analysis at Taiwan Semiconductor Manufacturing Co. He received B.S. from the University of Sao Paulo, Brazil and M.S. and PhD. from Stanford University; all are in Chemical Engineering. After leaving Stanford University, David taught in the Department of Materials Engineering at San Jose State University and then joined Philips Semiconductors in Sunnyvale-California before becoming Director of Focused Ion Beam and Transmission Electron Microscopy Development at Accurel Systems, Sunnyvale-California, USA. David Su is a member of the Materials Research Society, Microscopy Society of America, and the Electronic Failure Device Analysis Society.

Su, K. C. (3A.1, IC.8)
K. C. Su received the B.S. degree (1986) and M.S. degree (1988) in Electrical Engineering from National Cheng Kung University, Taiwan, ROC. Then, he joined United Microelectronic Corp. (UMC) and worked in process technology development division for over 10 years. He is currently focusing on reliability technology & methodology development. His main interests are reliability engineering, device engineering and logic technology development.

Suehle, John (4B.1)
John S. Suehle received his B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, in 1980, 1982, and 1988 respectively. In 1981 he received a Graduate Research Fellowship with the National Institute of Standards and Technology (NIST), Gaithersburg, MD. Since 1982 he has been working in the Semiconductor Electronics Division at NIST where he is Leader of the CMOS and Novel Devices Group. His research activities include failure and wear-out mechanisms of semiconductor devices, radiation effects on microelectronic devices, micro-electro-mechanical-systems (MEMS), and nanoelectronic devices. Dr. Suehle has published over 170 technical papers or conference proceedings and holds 5 U.S. patents. He serves on the Editorial Board of the IEEE Transactions on Electron Devices and has served as Guest Editor of the IEEE TDMR. Dr. Suehle served as General Chair of the 2008 International Reliability Physics Symposium and also serves on the management committees of the IEEE Integrated Reliability Workshop and the IEEE International Electron Devices Meeting. He is the chairman of the Oxide Integrity Working Group of the EIA/JEDEC JC 14.2 Standards Committee responsible for developing national standard test procedures for wafer-level reliability. He has also presented numerous tutorials on thin oxide reliability and is a Senior member of IEEE and a member of Eta Kappa Nu.

Sugawa, Shigetoshi (XT.9)
Shigetoshi Sugawa received his M.S. in 1982 in Physics from Tokyo Institute of Technology and his Ph.D. in 1996 in Electrical Engineering from Tohoku University. In 1982-1999 he worked in Canon Inc., where he researched high S/N ratio solid-state imaging devices, high performance amorphous silicon devices, high-speed low power SOI devices and high-density liquid crystal display devices. In 1999 he moved to Tohoku University and he is presently a professor at Graduate School of engineering, Tohoku University.

He is currently engaged in researches on CMOS image sensors, high-performance ULSI's and advanced displays such as high-performance, high-speed and low-power circuits/devices, and advanced semiconductor process technologies related to high-quality low-temperature oxidation, nitridation, CVD and etching process using microwave-exited high-density plasma. Dr. Sugawa is a member of the IEEE, the Institute of Image Information and Television Engineering of Japan.

Sugiyama, Yoshihiro (2E.4)
Yoshihiro Sugiyama received the B.S., M.S., and Ph.D. degrees in Electronic Engineering from Tohoku University, Sendai, Japan in 1982, 1985, and 2000, respectively. He joined Fujitsu Laboratories Ltd., Atsugi, Japan in 1985. From 1985 to 2000, he was engaged in research of quantum effect devices with III-V materials. Since 1999, he has started to research and develop silicon technologies including SiGeC, high-k gate dielectrics, ferroelectrics. His recent interests include Flash, ReRAM, FRAM, and STT-MRAM for SoC. Dr. Sugiyama is a member of the Japan Society of Applied Physics, and the Institute of Electronics, Information and Communication Engineers of Japan.

Sun, Q.Q. (XT.1)
Q. Q. Sun received his B.Sc. degree in Physics from Fudan University , Shanghai, China in 2004. He is currently working toward the PH.D. degree in Microelectronics and Solid State Electronics at Fudan University, Shanghai, China, mentored by Prof. David Wei Zhang. His research area is atomic layer deposition, high-k dielectrics for advanced MOSFET, and modeling of point defects in high-k dielectrics by first-principles calculation. He is also involved in development of novel back-end of line process.

Sunderland, David (2H.6)
David Sunderland received BS and MS degrees from the University of Missouri in 1977 and 1978, and the Ph.D. in 1987 from USC. He joined Hughes Aircraft in 1978, where he designed custom ICs for satellites. He joined IBM in 1989, and was responsible for device design, modeling and groundrules in bipolar, CMOS and BICMOS technologies. Since returning to Hughes (now part of Boeing) in 1996, he has been responsible for selection and qualification of high-performance, yet highly reliable and radiation-tolerant, semiconductor technologies for spacecraft applications. He is a Boeing Senior Technical Fellow.

Sune, Jordi (BD.6)
Jordi Suñé. Graduated in Physics in 1986 and PhD. in Electronics in 1989 both from the Universitat Autònoma de Barcelona (UAB). Research fellow at IMEC (1989) and at the University of Bologna (1990,1991). Full Professor of Electronics at the UAB since 2002. He has (co)authored more than 150 papers in international journals and relevant conferences, among which 11 International Electron Device Meeting (IEDM) papers, several invited papers and five tutorials on oxide reliability at the International Reliability Physics Symposium (2001, 2004, 2005, 2008 and 2009). He has served in the technical committees of IRPS, IEDM, INFOS, and SISC. He has received the Award of the Generalitat de Catalunya for the promotion of Research (2004) and the IBM Faculty Award (2008). Main fields of interest are gate oxide reliability and modeling and simulation of electron transport.

Sung, Suk-Kang (MY.3)
Suk-Kang Sung was born in Korea, in 1973. He received the B.S., M.S., and Ph.D. degrees from School of Electrical Engineering, Seoul National University, Seoul, Korea, in 1997, 1999, and 2004, respectively. Since 2004, he has been with Samsung Electronics Company, Ltd., Kyungki-Do, Korea. He has focused on nano-scale CMOS devices, Flash memories and future nonvolatile memories including SONOS, nano crystal memory. Currently, He joins the 64Gb NAND flash product development.

Suzuki, Ken (4A.6)
Dr. Ken Suzuki received M.S. and Ph.D degrees from Tohoku University in 1999, 2002, respectively. He has been working on the quantum molecular dynamics analysis for point-defect engineering of nano- and micro-scale materials and thin film devices. Now he is Assistant Professor of Fracture and Reliability Research Institute, Graduate School of Engineering, Tohoku University.

Sverdlov, Viktor (5D.2)
Viktor Sverdlov received his Master of Science and PhD degrees in physics from the State University of St. Petersburg, Russia, in 1985 and 1989, respectively. From 1989 to 1999 he worked as a staff research scientist at the V.A.Fock Institute of Physics, St.Petersburg State University. He visited ICTP (Italy, 1993), the University of Geneva (Switzerland, 1993-1994), the University of Oulu (Finland, 1995), the Helsinki University of Technology (Finland, 1996, 1998), the Free University of Berlin (Germany, 1997), and NORDITA (Denmark, 1998). In 1999, he became a staff research scientist at the State University of New York at Stony Brook. He joined the Institute for Microelectronics, Technische Universität Wien, in 2004. His scientific interests include device simulations, computational physics, solid-state physics, and nanoelectronics.

Sverdrup, Per (NA.1)
Per Sverdrup earned a Ph.D. in mechanical engineering from Stanford University in 2000 with a focus on microscale heat transfer. He joined Intel in 2000, working on interconnect self-heat/electromigration, junction/package temperature, and transistor aging modeling. He currently is working on System-on-a-Chip (SOC) design productivity initiatives.

Tack, Marnix (4C.2)
Marnix Tack received the M.Sc. degree in electrical engineering from the University of Gent, Belgium, in 1984, and the Ph.D. degree from the Catholic University of Leuven, Belgium in 1991. He joined IMEC in 1985 doing research on SOI-CMOS and cryogenic CMOS. In 1990, he joined Mietec, now ON Semiconductor, Belgium, managing the development of CMOS, BiCMOS, HV and NVM processes and design kits. Presently he is Director of the Power Technology Centre, focusing on the development of new High Voltage and Power Discrete and Integrated Semiconductor Technologies. He (co-)authored over 70 papers in the above fields.

Tahi, Hakim (EX.1)
Hakim Tahi received his Master degree in microelectronics from the University of Tizi ouzou, Algeria. In 2007, he joined the Microelectronics and nanotechnology Division of CDTA, Algiers, Algerea, where he works as research assistant on the electrical characterization of interface and oxide trap induced by radiation in MOS devices.

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Shinichi Takigawa was born in Kyoto, Japan, 1961. He received the B. S. and M. S. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1983 and 1985, respectively. In 1985, he joined Electronics Research Laboratory, Matsushita Electric Industrial Co., Ltd. (Panasonic), Osaka, Japan. Since then, he has been involved in the research and development of semiconductor devices. He is a member of the Institute of Electronics, Information and Communication Engineering (IEICE) of Japan.

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Kian-Ming Tan received the B.Eng. and M.Eng. degrees in electrical engineering from the National University of Singapore, Singapore, where he is currently working toward the Ph.D. degree in electrical engineering in the Department of Electrical and Computer Engineering. His research interests include plasma etching technologies, strained Si device, and fabrication of multiple-gate transistor.

Tanaka, Tsuyoshi (CD.5)
Tsuyoshi Tanaka (M'96) received the B.S. and M.S. degrees in applied physics from Osaka University, Osaka, Japan, in 1983 and 1985, respectively. He received Ph. D. degree in electronics engineering from Osaka University in 2000. Since 1985, he had been engaged in the research and development of compound semiconductor devices mainly for high frequency applications at Matsushita Electric Industrial Co., Ltd (Panasonic). At present, He serves as the director of Semiconductor Device Research Center, Semiconductor Company, Panasonic Corporation. His current research interests include GaN-based power transistors and laser diodes.

Tang, Chin-Hsin (6C.4)
Chin-Hsin Tang received the M.S. in electrical engineering from National Taiwan Ocean University in 1997. In 1997, he joined TSMC where he works on failure analysis (FA) of reliability failure devices and customer complaint case. He has had the FA experience of 0.5um, 0.35um, 0.25um and 0.15um Logic, 0.13um, 90nm and 65nm SRAM already. Currently, he is the Principal engineer for the failure analysis of 40nm SRAM.

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Chun-Jung Tang was born in Tainan, Taiwan, R.O.C., in 1982. He received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2004, where he is currently working toward the Ph.D. degree in electronics engineering. His main research interests are in the field of experimental characterization and reliability analysis in high-k devices and nonvolatile memories and Monte Carlo simulation.

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Augusto Tazzoli (IEEE Member) was born in Padova, Italy in 1978. He graduated in Electronics Engineering at the University of Padova in 2003. In March 2004 he received a Master in Information Security, and in 2006 the Ph.D. degree in Electronics and Telecommunications Engineering. He currently holds a post-doc position, working on RF-MEMS, ESD phenomena, and compound semiconductors. He has co-authored more than 50 papers (3 best papers). He serves as reviewer of international Journals (IEEE Electron Device Letters, Solid State Electronics, Transaction on Industry Applications, Microelectronics Reliability), and, since 2007, he is in the TPC of the "EOS/ESD Symposium".

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Thompson, William (3E.2)
William Thompson is currently the chief scientist for the Orion division of Carl Zeiss SMT. Previously Bill was director of engineering for the Schlumberger/NPTest Probe Systems division. Bill has also been R&D manager or chief scientist for Varian's ion implanter and e-beam lithography divisions, for IBT, a focused ion beam company, US product manager for JEOL's FIB and e-beam lithography systems and chief scientist for Micrion. At Micrion, Bill managed a DARPA & Sematech group responsible for building the first Gas Field Ion Source (GFIS) based mask repair system. Bill has a BS in physics from Dartmouth College and a PhD in experimental nuclear physics from Yale University.

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Tushar Thrivikraman received the M.S. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, in 2007, and completed a joint B.S. and B.B.A. degree from Georgia Tech and Emory University, Atlanta, GA, in 2002. He is currently a Ph.D. candidate at the Georgia Institute of Technology. He is a member of the Silicon Germanium Devices and Circuit Research Team at Georgia Tech, concentrating on the design of next-generation radar and communication modules. Prior to joining the Georgia Institute of Technology, he was a Defense Career Intern at the Robins Air Force Base, supporting radar systems.

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Anne-Katrin Tiedemann studied electrical engineering at the University of Wuppertal, Germany and received her diploma in 2005. Since 2006 she is a PhD student at the Department of Electronics of the University of Wuppertal. Her main research interest is micro and nano characterization of materials and devices by Scanning Thermal Microscopy and Scanning Electron Microscopy.

Tőkei, Zsolt (5A.4, IC.9)
Zsolt Tőkei is program director for the advanced interconnect program. He joined IMEC in 1999 and since then he is working in the field of copper low-k interconnects. He obtained his M.S. (1994) in physics from the University Kossuth in Debrecen, Hungary. In the framework of a co-directed thesis between the Hungarian University Kossuth and the French University Aix Marseille-III, he earned his PhD (1997) in materials science. From 1998 he worked at the Max-Planck Institute of Düsseldorf, Germany, as a post-doctorate researcher. In 1999, he joined the Interuniversity Microelectronics Center (IMEC), Belgium, where he has worked on a range of interconnect issues such as metallization, process development, electrical performance, interconnect scaling and dielectric reliability.

He has authored or co-authored more than 100 publications in international scientific journals and in international scientific proceedings.

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Gabriel Torrens received the M.S. degree in Engineering from the Polytechnic University of Catalonia in 2004. He is currently working towards his Ph.D. at the Electronic Systems Group of the Balearic Islands University. His research interests include VLSI design and radiation induced phenomena.

Tränkle, Günther (2C.2)
Günther Tränkle received his diploma degree in physics at the Technical University Munich in 1981 and his doctoral degree in physics at the University of Stuttgart in 1988, where he worked on quantization and many-body effects in III/V quantum well structures. In 1988, he joined the Walter-Schottky-Institute at the TU Munich, running its III/V-semiconductor technology and working on field-effect transistors and laser diodes. From 1995 to 1996, he was a Department Head at the Fraunhofer-Institute for Applied Solid-State Physics in Freiburg being responsible for the development and realization of electronic and optoelectronic III/V semiconductor devices. In 1996, he became head of the Ferdinand-Braun-Institute in Berlin. Since 2002 he also holds a chair on microwaves and optoelectronics at the Technical University Berlin. His current research interests include III/V-semiconductor technology, micro- and mm-wave devices and high power diode lasers. In the last years he has co-founded 5 start-up companies.

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Youssef Travaly holds a Ph.D. in Materials Science. He joined IMEC (Belgium) in 2000, where he currently works as Associate Program Manager. He has authored and co-authored about 100 papers in the field of semiconductors.

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Lorenzo Trevisanello received the degree of Electronics Engineering in 2005 and in 2006 he started his Ph.D. studies in Electronic and Telecommunication Engineering at the University of Padova. His research topics are the study of degradation mechanism induced by thermal and electrical stress on GaN LEDs and development of thermal characterization techniques.

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Fu-Yi Tsai received the Ph.D. degree in electronics engineering from National Chiao-Tung University, Taiwan, in 2001. He worked with Winbond Electronics, Hsinchu, Taiwan, on ESD protection design in 2004. Currently, he is working in Faraday Technology Corporation, Hsinchu, Taiwan, as the team leader on the topics of ESD protection design and signal integrity. Dr. Tsai has served as the member of Technical Program Committee in Taiwan ESD Conference since 2007.

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Koji Tsunoda received the B.S. and M.S. degree in Electronics Engineering from University of Tokyo, Tokyo, Japan in 1995 and 1997, respectively. In 1997, he joined Fujitsu Laboratories Ltd, Atsugi, Japan, where he has been engaged in research and development of embedded memory devices. He was also a visiting scholar at Stanford University, California from 2005 to 2006. His present activities include development of emerging memory devices, especially magnetoresistive random access memory.

Tu, Wen-Hsien (MY.4)
Wen-Hsien Tu received the B.S. degree in electronics engineering in 2007 from National Central University, Taoyuan, Taiwain, R.O.C.. She is currently pursuing the M.S. degree in electronics engineering from National Chaio-Tung University, Hsinchu, Taiwain, R.O.C.. Her research interest now focuses on the program/erase transient models and RTN impact forecast for the SONOS flash memory.

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Chih-Hang Tung (SM'02) received the M.S. degree in materials engineering from the Illinois Institute of Technology, Chicago, in 1987. He has worked at Electronics Research and Service Organization (ERSO), Industrial Technology Research Institute ITRI), Taiwan, R.O.C., and the Vanguard International Semiconductor Corporation. In 1996, he joined the Institute of Microelectronics (IME), Singapore, as a Senior Member of Technical Staff. His main research interests have been in the application of transmission electron microscopy in semiconductor materials, device and process characterization, DRAM and SRAM reliability and failure analysis, physical and chemical characterization of VLSI/ULSI process and products. He has published more than 100 journal and conference papers, and recently authored the book, ULSI Semiconductor Technology Atlas (New York: Wiley, 2003). Mr. Tung is a member of the organization committee and Technical Co-Chair of IPFA 2005.

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Stanislav Tyaginov was born in Leningrad (Saint-Petersburg), Russia in 1978. He received his MS degree in Physics (Saint-Petersburg Technical University) in 2002 and his Doctoral degree in Physics in 2006 (Ioffe Physical-Technical Institute). His PhD work was devoted to the problem of impact of insulator thickness non-uniformities on

MOS tunnel structure characteristics. He participated at the Samsung Summer Internship Program-2005 (South Korea). Starting from 2008, S.E. Tyaginov has been working for the Institute for Microelectronics, TU Wien as a post-doc researcher. His scientific interests include the modeling of HCI-related degradation and TDDB as well as tunneling phenomena in MOS devices.

Ueda, Shigenori (4A.6)
Dr. Shigenori Ueda has been working on magnetic meterials, strongly-correlated sysytem, and X-ray Photoemission Spectroscopy with SR X-rays in RIKEN from 2000 to 2005 and in Japan Synchrotron Radiation Research Institute (JASRI) from 2005 to 2006. Now he is Researcher of National Institute of Materials Science, Japan.

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Hiroki Usui received the B.S (1989) and M.S. (1991) in Electronic Engineering from Tokai University, Kanagawa, Japan. He joined SONY Corp. in 1991. He is a senior manager of the product reliability engineering in advanced CMOS and packaging technology. His current engineering interests are realistic reliability modeling for soft error, transistor and packaging reliability. He is a member of the IEEE.

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Balaji Vaidyanathan recieved his B.E. (2003) from University of Madras, India. He is currently pursuing his Ph.D. in computer science and engineering from PennState University. He joined R&D Division of TSMC in 2007 as an engineer and is responsible for digital/analog/RF circuit NBTI and PBTI aging assessment.

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Maria Grazia Valentini received the Laurea degree in physics from Milan Univesity, Italy, in 1982. Since 1983, she has been with STMicroelectronics, Agrate Brianza, Italy, working with the Technology Diffusion Group. Since 1997, her research interests have focused on transistor and metallization reliability issues. In 2008 she joined Numonyx, maintain the same role.

van de Wel, Paul (5E.2)
Paul van der Wel is working for 13 years in the field of reliability. First 3 years at Akzo Nobel on the reliability of electro- and thermal optical switches. Since 1999, he works at NXP Semiconductors, formerly known as Philips Semiconductors. He covers a wide area of technologies with the emphasis on RF and MEMS.

Van Houdt, Jan (2A.5)
Jan Van Houdt started at IMEC in 1988 and received the Ph.D. degree from the Katholieke Universiteit Leuven in 1994. During his PhD work, he invented the HIMOS™ Flash memory, which was transferred to several industrial production lines. In 1999 he became responsible for the Flash memory activities at IMEC and as such was the driving force behind the expansion of IMEC's memory program, currently joint by all major memory companies. Today he is IMEC's Memory Device Manager. He has published more than 140 papers in international journals, wrote 2 book chapters and accumulated more than 120 conference contributions (including 20 invited papers and panel contributions). He has filed about 45 patent applications worldwide in the area of memories and served on the program committees of 7 major conferences.

Vashchenko, Vladislav (6C.1)
Dr. Vladislav Vashchenko received MS, Engineer-Physicist (1986) followed by "Ph.D. in Physics of Semiconductors" (1990) from Moscow Institute of Physics and Technology for the study of self-organization phenomena in semiconductor structures under breakdown and injection. He worked then as an engineering manager in reliability department of State Research Institute "Pulsar" (Moscow). He was awarded the highest doctorate degree in Russian Federation "Doctor of Science in Microelectronics" (1997) (similar to Habilitation in Germany) for the cycle of studies of physical limitation of safe operating area in discrete power and microwave GaAs and Si devices, developed test methods for local structural defects detection and solutions of the reliability problems.

Verma, Gautam (3A.2)
Gautam Verma is with Altera Corp since 2005 as Senior Member Technical Staff in the Customer Quality group. Previously, he worked at Intel Corp for more than 20 years in several different areas of Quality and Reliability. In 1988, he received an Intel Achievement Award for his work in the development of Flash memory technology. Dr. Verma also served as Intel assignee to Sematech during 1990-1992. Dr. Verma received his PhD in Physics from University of Southern California, Los Angeles, on low-temperature conduction properties of quasi one-dimensional compounds.

Vermeire, Bert (2G.4)
Bert Vermeire is an associate research professor of Electrical Engineering at Arizona State University. He directs the Wireless Integrated and Nanotechnology research center at ASU. His research interests include electronics for precision instrumentation and their operation in harsh environments.

Verzellesi, Giovanni (CD.4)
Giovanni Verzellesi was born in Italy in 1964. He received the "Laurea" degree (Univ. of Bologna) and the PhD (Univ. of Padova) in Electrical Engineering in 1989 and 1994, respectively. From 1994 to 1999, he was with the University of Trento, Italy, as a Research Associate. In 2000 he joined the University of Modena and Reggio Emilia. In 2001 he was appointed Associate Professor of Electronics, and, since Sept. 2006, he has been a Full Professor of Electronics at the same university. His research activity has covered: (i) impact-ionization effects in silicon BJTs; (ii) silicon optical and chemical sensors and radiation detectors; (iii) III-V and GaN FETs.

Vilmay, Maxime (6A.2)
Maxime Vilmay received the enigineer degree in Material Science form the Ecole Nationale Supérieur ed'Ingénieur de Caen (Caen, France) in 2006 and the M.S degree in Material Science from University of Caen (France) in 2006. He is currently working with STMicroelectronics toward the PhD degree. His research focuses on low- k dielectrics reliability for advanced technology nodes.

Visconti, Angelo (3C.1)
Angelo Visconti member of Numonyx Technical Staff, received the Laurea degree in physics, cum laude, from the University of Milano at Como, Italy, in 1997, writing his thesis on the feasibility of optical temporal solitons in quadratic nonlinear materials. Beginning in 1987, he worked ten years as a hardware and software designer and project leader for industrial automation systems. In 1997, he joined the Non-Volatile Memory Process Development Group, Central Research and Development department of STMicroelectronics (now Numonyx), Agrate Brianza, Milano. His first activities were about the study and characterization of channel erase, CHE programming currents and SILC phenomena in Flash cell. Since then, he was involved in the developments of 0.25-0.041 mm CMOS High Density Flash Memory Process. In particular, he was involved in the development of NOR and NAND multilevel Flash devices. His present main interests are on reliability, radiation effects, and multilevel applications of Flash cells, in both NOR and NAND array architectures. He is author, or co-author, of more than 80 publications and 12 patents in the non-volatile memory field and nonlinear optical field. He is the Numonyx-scientific responsible for research projects, on radiation effects and reliability phenomena, with Padova and Milano Universities. He is a Lecturer on Non-Volatile Memory Reliability and Radiation Effects on Flash Memory at University of Padova and Politecnico di Milano. Since 2005, he has been the ST-rapresentative within the JEDEC sub-committee on NVM reliability.

He was a member of the IEDM-CIR committee in 2005 and 2006 and had chaired the IEDM CIR-NVM memory sessions in 2005 and 2006, also member of IRPS-PIR committee in 2007 and, finally, member of IPRS-Memory Reliability committee in 2008 and 2009.

Vollertsen, Rolf-Peter (BD.6, XT.6)
Rolf-Peter Vollertsen received his doctoral degree (Ph.D.) in 1987 in material science engineering from the University of Erlangen, Germany. After joining Siemens AG in Munich, Germany he focused on thin single and multi layer dielectric reliability. He worked ten years in the DRAM Development Alliance at the IBM Microelectronics Division site in Essex Junction, Vermont (USA), where he collected experience in device and product reliability. Dr. Vollertsen works for Infineon Technologies's central technology reliability department in Munich, Germany, on fast wafer level reliability test and methodology development. His focus is on reliability assessment of dielectrics and devices.

Wakiyama, Kuniko (6C.2)
Kuniko Wakiyama joined Sony Corporation, Tokyo, Japan in 1974, where she became involved in developing silicon MOS devices as technical assistant. Since 2007, she has been involved in developing ESD protection devices for high-voltage MOS ICs.

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Steven V. Walstra (S'90–M'98) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1992, 1994, and 1997 respectively. He joined Intel Corporation in 1998, and now manages the Reliability and Statistical Modeling area within the Design and Technology Solutions group. He has been a key developer and project leader for numerous CAD projects, including transistor degradation modeling, soft error modeling, oxide wearout, and ESD simulation.

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Mingxiang Wang (M'07) received the B.S. degree in Physics and Ph.D. degree in Condensed Matter Physics from Nanjing University, Nanjing, China, in 1993 and 1998, respectively. From 1998 to 2001, he was a Postdoctoral Research Associate with the Department of Electrical and Electronic Engineering, the Hong Kong University of Science and Technology, Kowloon, Hong Kong. Afterwards, he joined Semiconductor Manufacturing International Corporation, Shanghai as a member of technical staff in process reliability engineering. He is currently with the Department of Microelectronics, Soochow University, Suzhou, China. His research interests include thin-film materials and devices, semiconductor device physics and device reliability.

Wang, Ping-Chuan (5A.2)
Ping-Chuan Wang is currently with the Technology Reliability Dept. at IBM Microelectronics in East Fishkill, New York. He received his doctoral degree in materials science from Columbia University in 1997. After an appointment as a visiting scientist at Lehigh University, he joined IBM in 1997 and has been working on semiconductor technology reliability topics including BEOL and FEOL areas.

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Szu-Yu Wang was born in Kauhsiung, Taiwan in 1974. He received his B.S and M.S degrees in material science and engineering from National Tsing-Hua University (NTHU) in 1996 and 1998, respectively, and the Ph. D degree in electronic engineering from National Tsing-Hua University (NTHU) in 2008. He joined Technology Development Center in Macronix International (MXIC) since 2000. His current work is focused on technology development in nitride trapping Flash Memories.

Wang, Tahui (2B.4, MY.4)
Tahui Wang (S'84-M'85-SM'94) was born in Taoyuan, Taiwan, R.O.C., on May 3, 1958. He received the B.S.E.E. degree from National Taiwan University, Taipei, Taiwan, in 1980, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana–Champaign, Urbana, in 1985. From 1985 to 1987, he was with Hewlett-Packard Laboratories, Palo Alto, CA, where he was engaged in the development of GaAs HEMT devices and circuits. Since 1987, he has been with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, where he is currently a Professor. His research interests include hot-carrier phenomena characterization and reliability physics in very large scale integration (VLSI) devices, RF CMOS devices, and nonvolatile semiconductor devices. Dr. Wang was given the Best Teacher Award by Taiwan's Ministry of Education. He has served as technical committee member of many international conferences, among them International Electron Devices Meeting, International Reliability Physics Symposium, and VLSI Technology, Systems, and Applications.

Watabe, Shunichi (XT.9)
Shunichi Watabe was born in Japan, on September 9, 1982. He received the B.S. degree in electronic engineering and M.S. degree in management of science and technology both from Tohoku University, Sendai, Japan in 2005 and 2007, respectively. He is currently working toward the Ph.D. degree in the Graduate School of Engineering, Tohoku University. His research interests are the development of device and fabrication processes to suppress the variability of characteristics in MOSFETs.

Wen, Shi-Jie (FF.1)
Shi-Jie Wen received his Ph.D in Material Engineering from University of Bordeaux I in 1993. He joined Cisco Systems Inc., San Jose, CA in 2004, where he has been engaged in IC component technology reliability assurance. His main interest is in silicon technology reliability, such as SEU, WLR, and complex failure analysis, etc. He is a member of DFT, SEU core teams in Cisco. Before Cisco, he worked in Cypress Semiconductor where he was involved in the area of product reliability qualification with technology in 0.35u, 0.25u, 0.18u, 0.13u and 90nm.

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Christopher J. Wilson received the M.Eng. degree (first class honours) from Newcastle University, Newcastle upon Tyne, U.K., in 2006, where he is currently working toward the Ph.D. degree on interconnect reliability and mechanical stress in thin films in the School of Electrical, Electronic, and Computer Engineering, under the framework of the flagship EU FP6 project PULLNANO. Mr.. Wilson was recently Marie Curie APROTHIN Fellow and Visiting Scholar in the Advanced Interconnect Program at the Interuniversitair Micro-Elektronica Centrum (IMEC) for 16 months. He is an Institution of Electrical Engineers Robinson Research Scholar and holds an Institution of Electrical and Electronic Engineers Reliability Society Scholarship.

Wise, Rick (2C.4)
Rick Wise received the B.S. degree in chemical engineering from the University of Arkansas, Fayetteville, in 1983, and the M.S. and Ph.D. degrees in engineering and applied science from Southern Methodist University, Dallas, in 1987 and 2000, respectively. He has been with Texas Instruments, Dallas since 1983. He currently works in external research & consortia projects for the Analog Technology Development group. He was elected Texas Instruments Fellow in 1998. He has 17 issued U.S. patents and has authored or co-authored over 80 papers in journals and conference proceedings. Dr. Wise is a member of the Electrochemical Society and Tau Beta Pi. He has served on numerous technical advisory boards.

Wraback, Michael (2D.2)
Dr. Michael Wraback received his Ph.D. in physics from Brown University. He is currently the team leader of the Nitride Semiconductor Optoelectronics Team in the Microphotonics Branch of the EO&P Division of SEDD, presiding over research and development of semiconductor ultraviolet and visible light sources and detectors, high efficiency full-spectrum solar cells, and eye-safe optical generation and detection of terahertz radiation. He has authored or coauthored more than 200 papers and presentations addressing the physics of semiconductor materials and devices.

Wrachien, Nicola (2D.5, 2D.6)
Nicola Wrachien was born in Treviso, Italy, in 1982 and received the degree in Electronic Engineering after 5 years of University courses from the University of Padova (Italy) on July 2006 with magna cum laude. At Present he is a PhD student at the Department of Information Engineering – University of Padova, Italy. His research interests are reliability and ionising radiation effects on novel types of non volatile memories; reliability and electrical characterization of organic thin-film-transistors. He is author or co-author of some publications in international journals and conferences.

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Wu, Kenneth (3A.2, 4C.3, 6A.4, 6C.4, BD.3, IC.13)
Dr. Kenneth Wu is the Director of Technology Quality & Reliability at Taiwan Semiconductor Manufacturing Company (TSMC), responsible for technology reliability characterization and qualification. Prior to join TSMC in 2002, Dr. Wu worked at Intel Corporation since 1982 in technology development and reliability qualification. Dr. Wu has published more than 35 papers on a variety of technology and reliability subjects; and received IRPS The Best Paper Award in 1990. Dr. Wu received his B.S from National Taiwan University in 1975, an M.S. from Northwestern University in 1978 and his Ph.D. from Princeton University in 1982; all are in Electrical Engineering.

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James Ziegler is a Professor of Physics and Engineering at the United States Naval Academy (USNA) in Annapolis, MD, USA. He published the first work on the effects of cosmic rays on terrestrial electronics in 1979. His work on the stopping and range of ions in matter received 798 scientific citations in 2007. He is a Fellow of the American Physical Society and also of the IEEE.

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Nian-Kai Zous received the Ph.D. degree in electronics engineering from National Chiao-Tung University (NCTU), Hsin-chu, Taiwan, R.O.C., in 2002. He joined the Macronix International Co., Ltd. (MXIC) in Hsinchu, Taiwan, in 2003, working in the advanced device group of the Device Technology Division and his research activities include the study of reliability and scaling issues in nitride storage devices. From 2005 to 2007, he is working in the NBIT Flash Tech. Dept. II of MXIC and is responsible for the reliability issue on NBIT product. Since 2007, he has been engaged in the methodologies for technology development and yield enhancement .