Understanding Design Annotation

Summary

This application note explores the process of annotation in Altium Designer – from understanding Schematic, Board Level and PCB Annotation, maintaining design synchronization, to an in-depth coverage of annotating a multi-channel design.

Annotation is a routine task that designers have to perform to detail their work and maintain synchronization between different parts of their design. While Altium Designer allows you to automate this process with a single click, this application note explains the underlying nuts and bolts of annotation and provides information on driving it to help you fully leverage the various annotation capabilities.

Annotation in general is *the process of making critical or explanatory notes for the purpose of clarifying details*. More specifically, it is the systematic and methodical process for ensuring that each component is uniquely identified. Based on a component's designator, annotation is the primary means of referencing each component, both the logical component in the Schematic and the physical component on the PCB.

Annotation makes it possible to ensure that all the Schematic components remain related to their physical PCB implementation. PCB layout changes can result in a reassignment of designators or re-annotation, and these changes must be passed back to the Schematic environment. Each update has to be handled, tracked and verified, otherwise the components' designators and other design data can become out of sync.

Annotation in Altium Designer

There are three approaches to annotating your design:

1. Schematic Level Annotation – the annotation of the Schematic components in your design
2. Board Level Annotation – the annotation of board level (compiled) components in your design
3. PCB Annotation – the annotation of the PCB components in your design.

These three types of Annotation are graphically represented below.

Figure 1. Schematic and Board Level Annotation are performed in the Schematic Editor Environment. The Schematic Editor Environment consists of the Editor view where Schematic Level Annotation is performed, and the Compiled Documents View which shows compiled data (physical names of components), where Board Level Annotation is performed. The Compiled Documents view has options to show the source data (logical names) in superscript.

Which Annotation Tool?

Your choice of Annotation Tool depends on a number of factors including your design, personal preference and your company policy and procedures.

Schematic Level Annotation involves the systematic annotation of parts in your Schematic Design (logical design). It is useful when you have a simple design that is flat or hierarchical and does not use *Device Sheets*. Schematic Level Annotation allows you to specify the Order of Processing and Complete Existing Packages for multi-part components based on your chosen Component Parameters.

You can also use Schematic Level Annotation for multi-channel designs, which utilizes a default naming scheme which is specified in the **Multi-Channel** tab in your *Project Options*. The naming scheme in the **Multi-Channel** tab consists of Room Naming Style and Designator Format and can be customized based on a number of available keywords.

Note that Schematic Level Annotation is a prerequisite to Board Level Annotation, ensuring that multi-part components are packaged and each component has unique identifier.

Board Level Annotation involves annotating the compiled components (the physical view of your components) of your design through the Schematic Editor. Board Level Annotation can be used for all of your designs but is especially useful for multi-channel designs as it allows you to control the annotation of each channel, overriding the default naming in your *Project Options*.

Board Level Annotation is required for designs that include *Device Sheets*, enabling them to be incorporated into your design. In this way, you can re-annotate your whole design without actually modifying the original Device Sheet.

Board Level Annotation also resolves any conflicting annotation problems that may occur due to duplicate designators across your project, saving the changes to a `*.Annotation` text file. Board Level Annotation settings are remembered when you close your project and re-applied when you open and compile your project. Board Level Annotation also includes some additional keywords for naming schemes and allows you to apply naming schemes to all or selected parts or even apply a custom name to specific parts.

PCB Annotation is useful when your preference is to work in the PCB Editor, systematically assigning designators based on their position on the board. This Annotation Tool is also useful when it is not possible to have the Schematic and the PCB open at the same time.

Figure 2. Schematic Level Annotation is required before you can perform either Board Level Annotation or PCB Annotation. Your choice of Annotation Tool is driven by aspects of your design and personal preferences for naming your components.

In summary, initially perform **Schematic Level Annotation** to:

- Package your Multi-Part Components
- Annotate components based on their position in the Schematic Design
- Annotate your Multi-Channel designs using the default naming scheme as specified in your Project Options
- Prepare your design for additional annotation.
- Perform Board Level Annotation to:
- Annotate the compiled components in Device Sheets
- Uniquely name all of your components across all of your channels using naming schemes which include positional annotation using a Global Index and other configurable options
- Manually name your components
- Perform PCB Annotation to:
- Annotate components based on their position on the board in the PCB Design.

Schematic Level Annotation

The **Annotate Schematics** command allows you to systematically assign designators to all or selected parts in selected sheets of your current project, ensuring designators are unique and ordered based on their position. You can customize your annotation to package multi-part components, set Index and Suffix options, Reset Schematic Designators including any duplicate designators and Back Annotate from PCB. To *Annotate Schematics in* your project:

- Use the **Tools » Annotate Schematics** command which brings up the *Annotate* dialog

- The left hand side of the dialog is for configuring the Order of Processing, setting Matching Options for multi-part components and setting the scope of annotation including setting an Index and adding a Suffix for designators per Schematic Sheet
- The right hand side has the Proposed Change List including Current and Proposed Designators with the option to lock both the designator and the sub-part to exclude them from annotation.

The controls in the *Annotate* dialog are described in more detail below.

Order of Processing

Positional annotation is directed through the **Order of Processing** control. As you select one of each of the four positional annotation methods available, the graphical representation dynamically updates to illustrate how the components will be annotated.

Figure 3 shows the **Order of Processing** set to **Across Then Down**.

In this mode, scanning will start at the top left of the schematic sheet and move left to right until all components are designated. Choose from Across Then Down, Up Then Across, Down Then Across and Across then Up.

Positional annotation is based on the location of the component's designator. If your positional annotation is not performing according to your expectations, ensure that the designators are positioned correctly.

Figure 3. Order of Processing allows you to control annotation based on the position of components

Schematic Sheets to Annotate

You can annotate the designators for all or selected Schematic Sheets within the current project. Enable or disable the checkbox before the Schematic Sheet name to include or exclude the sheets from annotation.

Annotation Scope

Set your Annotation Scope, choose from one of the following:

- **All** – All parts in the Schematic Sheet will be annotated
- **Ignore Selected Parts** – All parts except those selected will be annotated
- **Only Selected Parts** – Only the parts selected will be annotated

Note: Parts to be excluded or included in Annotation need to be selected before you open the *Annotate* dialog.

Order of Annotation

- Configure the order in which the Schematic Sheets are to be annotated using the Order field. Type the Order directly into the field or use the arrows which appear once you click in the field to scroll to your preference.

Start Index

- Enable the Start Index checkbox and choose a numerical value to start the numbering from. For example, if you choose a Start Index of 100 and your first Designator is C?, it will be annotated to C100, the next C101 and so on.

Figure 4. The Part ID for each designator and sub-part of a multi-part component (U11 has 4 sub-parts) can be locked.

Suffix

- Choose a Suffix you wish to append to your designator. Alpha (A, B, C…) numerical (1, 2, 3…) and non numerical (_ * . %...) suffixes are supported including a combination of these.

Proposed Change List

The **Proposed Change List** displays the effect of every annotation option selected for your design before you commit to the changes. Click on the **Update Changes List** button to load your proposed changes into this list. If you are re-annotating, click

on the **Reset All** button to reset either all or duplicate designators and then click on the **Update Changes List** button to load your proposed changes into this list.

The **Proposed Change List** shows a list of all designators for the parts contained within the sheets selected for annotation. For each entry, there are details of the *Current* and *Proposed Designator* including *Sub* (part) and the *Location of the Part.*

The check box adjacent to the current designator allows you to **lock** specific designators. The check box adjacent to the current **Sub** column allows the Part ID for that sub-part to also be locked, preventing the swapping of incompatible parts in a multi-part component. Note that you can also set locking options for any component in its *Component Properties* dialog.

Use the **Reset All** button to reset all of the proposed changes for designators to the default Component Prefix, for example R?, C?, D?, U?, etc... You will be prompted with the number of changes that are made from the previous state and the original state before they are applied. After confirming the reset, the changes are displayed in the Proposed Designator column as shown below in Figure 5.

*Figure 5. The first dialog shows the Proposed Designator Change List before any changes are made. The second Proposed Designator change list is shown after the **Reset All** (designators) command has been applied.*

After reviewing proposed changes, click the **Accept Changes (Create ECO)** button. The *Engineering Change Order* dialog will appear, listing the proposed changes as modifications with a modification category, **Annotate Component**. Use this dialog to validate, report and execute the ECO, completing the Annotation Process at the Schematic level.

Matching Options for Annotating Multi-Part Components

Matching Options allows for easier initial packaging of un-annotated multi-part components and the addition of new parts to existing multi-part components. **Matching Options** are especially designed for ease of grouping multiple parts into their correct physical components.

Primary considerations for annotating multi-part components are how those components will be matched and grouped together, what criteria will be used for grouping them and how much control you will have over the process.

*Figure 6. **Matching Options** are designed for grouping multi-part components for annotation.*

Complete Existing Packages

To configure your Matching Options, first select how you would like to **Complete Existing Packages**. This control lets you decide how and if parts that are not annotated will be included in existing packages.

Choose from:

- None – existing packages will not be completed and all new parts will be placed into new packages

- Per Sheet – existing packages will only include new parts from the same Schematic Sheet
- Whole Project - existing packages will include new parts from any of the Schematic Sheets in your project.

Component Parameters

Select the **Component Parameters** to package your components by. The default settings in the *Annotate* dialog are to complete existing packages by *Library Reference* and *Comment*. A **Component Parameter** helps you identify and match multi-part components based on common properties. The parameters listed reflect all of the parameters available across the components in the design. These are defined in the **Parameters** region of the *Component Properties* dialog.

Selecting any parameter in this column means that you will be using this parameter to match your parts into packages. If multi-part components share the enabled parameters and a common value, then they will be packaged together.

For example, in Figure 7, there are 8 OR Gates and 8 resistors. The OR gates contain a parameter called *QuadOrGate*, with one group of 4 OR gates having the parameter value, `Package1` and the other group of 4 OR Gates having the parameter value, `Package2`. The resistors have no such parameter. Enable the checkbox for *QuadOrGate* in the **Component Parameter** control to use this parameter to control how the components are packaged, in this case, the *Strictly* check box is not enabled.

After launching **Tools » Annotate Schematics**, parts with the parameter, *QuadOrGate=Package1* are packaged into the same physical component and those that have the parameter, *QuadOrGate=Package2* are also packaged together separately.

Any remaining components which do not have the *QuadOrGate* parameter are packaged together. In this case, the resistors are packaged together as their common attribute is that they do not contain the *QuadOrGate* parameter.

Figure 7. The OR Gates are packaged together based on the QuadOrGate parameter. The resistors are also matched and annotated as if they are a single packaged component (R1A, R1B, R1C, etc.) because their common attribute is that they do not contain the QuadOrGate parameter.

Strictly

If the **Strictly** checkbox is enabled for a Component Parameter, all components *must* have that parameter to be matched into a package. Components that do not have this parameter are annotated as individual components and are not packaged. This is illustrated in Figure 8 using the same example as above.

*Figure 8. The OR Gates are packaged together based on the QuadOrGate parameter which is enforced **Strictly**. Notice that the resistors are annotated as individual components (R1A, R2A, R3A etc) rather than packaged. **Strictly** means that the component must contain this parameter to be packaged.*

Keep in mind that enabling **Strictly** requires that all components throughout the entire design have this parameter in order to be packaged, so you would typically disable **Strictly**.

Preventing Part Swapping during Annotation

You can prevent the unpackaging or swapping of component sub-parts during annotation at the component level through the *Component Properties* dialog and the **SCH Inspector** (Lock Part ID). Enable the **Locked** checkbox in the *Component Properties* dialog as shown in Figure 9. To use this option selectively within a multi-part component, enable it once the component is placed on the Schematic Sheet.

Enable it in the **SCH Library Editor** if you want all sub-parts of that component to always have the **Locked** check box enabled. In addition, you can lock designators and sub-parts in the *Annotate* dialog.

Figure 9. You can lock the sub-part of a component in the Component Properties dialog in the Schematic Editor.

Alpha or Numeric Multi-Part Component Annotation

Multi-part components can use either an alpha or numeric part identifier suffix, for example, U1:1, U1:2 or U1:A, U1:B. You can control the style of suffix in **Tools » Schematic Preferences** in the **General** tab under the **Schematic** folder. Note that it is a global environment option and applies to all currently open Schematic Sheets.

Figure 10. The multi-part component suffix can be either Alpha or Numeric.

Reporting Unused or Duplicate Parts

There is an option for generating a report for unused or duplicate sub-parts upon compilation. Enable the options in the **Error Reporting** tab of the *Project Options* dialog.

Figure 11. Enable the Error Reporting Mode to detect any unused sub-parts in your design.

Reset Schematic Designators

*Figure 12. An additional level of control in the **Reset All** drop-down combo allows you to reset all or reset only duplicate designators in your design.*

Before you reset your designators, ensure that one of the source Schematic Documents is open and active in the main design window.

You can Reset Schematic Designators from the *Annotate* dialog using the **Reset All** button. An additional level of control allows you to either Reset All or *Reset Duplicates.* Reset Schematic Designators resets all of the component designators for the selected Schematic Sheets in the active project to the default component prefix, E.g. R?

You can also reset your designators using the **Tools » Reset Schematic Designators** command. Only the components in the Schematic Sheets selected in the *Annotate* dialog will be reset. Note that any designators with a locked status are not reset or changed in any way.

After launching the command, any source Schematic Documents that are currently closed will be opened and hidden and a confirmation dialog appears. This dialog summarizes the number of designators requiring an update and asks whether you wish to proceed with the changes. After clicking **Yes**, all component designators across all selected Schematic Sheets of the active project will be reset, appearing in the format: R?, C?, D?, U?, etc., as shown below.

*Figure 13. **Tools » Reset Schematic Designators** resets these component designators to the format U?A, U?B, U?C,U?D, C?.*

Reset Duplicate Schematic Designators

You can Reset Duplicate Designators from the *Annotate* dialog using the **Reset All** button. Click on the drop-down of the **Reset All** button and select **Reset Duplicates**.

You can also reset duplicate designators using the **Tools » Reset Duplicate Schematic Designators** command. This command resets duplicate designators, for example, if two capacitors have the same designator C8, one of them will be reset to C? when this command is used. Only the components in the Schematic Sheets selected in the *Annotate* dialog will be reset. Note that any designators with a locked status are not reset or changed in any way.

Annotate Schematics Quietly

You can **Annotate Schematics Quietly** through the **Tools** menu, giving you the ability to make a one-click annotation of the design without having to go through the *Annotate* dialog. This command is driven by the *Annotate* dialog and will obey any settings you have specified there, including Schematic Annotation Configuration settings such as **Matching Options**. If you have already configured your Annotation settings ahead of time, you can use this commands through the **Tools** menu. Annotation is then handled quietly in the background.

The **Tools » Annotate Schematics Quietly** command assigns a unique designator to any component whose designator is in the reset state (R?, C?, etc.), without launching the *Annotate* dialog. It does not assign a unique designator for duplicates.

*Figure 14. **Annotate Schematics Quietly** and **Force Annotate All Schematics** commands are available the **Tools** menu*

Force Annotate All Schematics

*Figure 15. A prompt informs you how many designators will be updated when **Tools » Force Annotate All Schematics** is launched.*

Similarly to Annotating Schematics Quietly, this command is driven by the *Annotate* dialog and will obey any settings you have specified there. If you have already configured your Annotation ahead of time, you can use this command through the **Tools** menu.

To re-annotate all component designators in accordance with the positional annotation scheme defined in the *Annotate* dialog, use the **Tools » Force Annotate All Schematics** command.

You will be prompted as shown (Figure 15) before the annotation is completed. Annotation is then handled quietly in the background.

Back Annotate Schematics

You can Back Annotate from PCB to the Editor View (the logical Schematic design) in Schematics through the *Annotate* dialog using the **Back Annotate** button. You can also Back Annotate your logical schematic design using the **Tools » Back Annotate Schematics** command. This command updates the designators of components in the Schematic Sheets of the active project with changes made in the PCB document. These changes are applied using a WAS-IS file that is generated when re-annotating designators in the PCB environment.

The feature is useful when it is not possible to have the schematic and PCB open at the same time, for example, when they are being designed by different people in different locations. Otherwise, it is best practice to use **Design » Update** to push annotation changes from the PCB back to the schematic.

Number Schematic Sheets

You can number your Schematic Sheets using the **Tools » Number Schematic Sheets** command. This function enables you to uniquely number Schematic Sheets.

Figure 16. The Number Schematic Sheets dialog.

Auto Sheet Number

Click on the **Auto Sheet Number** drop down combo to choose your Schematic Sheet Numbering Options.

Select Numbering Scheme

- **Display Order**: The sheets are numbered in the order they are displayed
- **Sheets Hierarchical Structure – Depth First**: The sheets are numbered from the top level into each branch. The top level is numbered first and then the first branch under the top level is numbered completely, the second branch and so on.
- **Sheets Hierarchical Structure – Breadth First**: The sheets are numbered according to their level in the hierarchy. Top level is numbered first, all second levels are numbered next and so on.

Select Numbering Method

Choose from an **Increasing** or **Decreasing** numbering method for your Schematic Sheets.

Numbering Schematic Sheets

After selecting your Numbering Scheme and Numbering Method:

- Click the **Auto Sheet Number** button, the **SheetNumber** column will be updated to match your selections
- Click **OK** to accept your changes or choose to customize your **Document Number**.

Auto Document Number

Click on the **Auto Document Number** drop down combo to choose your Document Numbering Options.

Select Numbering Scheme

- **Display Order**: The sheets are numbered in the order they are displayed
- **Sheets Hierarchical Structure – Depth First**: The sheets are numbered from the top level into each branch. The top level is numbered first and then the first branch under the top level is numbered completely, the second branch and so on
- **Sheets Hierarchical Structure – Breadth First**: The sheets are numbered according to their level in the hierarchy. Top level is numbered first, all second levels are numbered next and so on.

Select Numbering Method

Choose from an **Increasing** or **Decreasing** numbering method for your Documents.

Parameters

- **Prefix** - choose a prefix to affix in front of your Document Number. Alpha (A, B, C…) numerical (1, 2, 3…) and non numerical (_ * . %...) postfixes are supported including a combination of these
- **Start** - choose a numerical value to start your Document Numbering from
- **Postfix** - choose a postfix to append to your Document Number. Alpha (A, B, C…) numerical (1, 2, 3…) and non numerical (_ * . %...) postfixes are supported including a combination of these
- **Step** – choose a value to step up your Document Number by. For example, if you set your **Start** index to 1 and you set this **Step** value to 100, your first Document Number will be 1 and your next Document Number will be 101 (`Start + Step`), he next one will be 201 and so on.

Update Sheet Count

Click on the **Update Sheet Count** button to revise the Sheet Count for the current project. The Sheet Count is the total number of sheets in the project, regardless of your Numbering Scheme.

Move Up / Move Down

Use the **Move Up** or **Move Down** buttons to change the order in which the Schematic Sheets are displayed. This is relevant when you choose to customize your **Sheet Number** or **Document Number** using the **Display Order** Numbering Scheme.

Custom Numbering/Naming of your Schematic Sheets

You can create custom names or numbering for your Schematic Sheets by typing directly into the **SheetNumber** and/or **DocumentNumber** field. You can use any combination of alphanumeric or non-alphanumeric characters. After entering your custom names, click **OK** to implement your custom annotation.

Using Sheet Numbers and Document Numbers in your Project

Once you have configured your **Sheet Numbers** and **Document Numbers**, place the `SheetNumber` or `DocumentNumber` special string in your project to reference this information:

- Ensure that you have **Convert Special Strings** enabled in **DXP » Preferences » Schematic » Graphical Editing**
- Place a special string where the value `=SheetNumber` or `=DocumentNumber`. You can use Special Strings in values of Parameter Properties, Text Strings, Net Labels

etc.

For more information on Special Strings, refer to the *Schematic Editor and Object Reference*.

Schematic Sheet Numbering and Device Sheets

Sheet or Document Numbers cannot be configured for *Device Sheets* when they are read-only (default state). Device Sheets are cross hatched in the *Sheet Numbering* dialog to indicate their read-only state. When Device Sheets are editable, the cross hatching is removed and Sheet and Document Numbering can be configured.

Board Level Annotation

Board Level Annotation is the process of annotating the compiled components (the physical view of your components) of your design through the Schematic Editor. **Board Level Annotate** allows you to either name your components based on a number of Naming Schemes, Back Annotate from PCB documents to the Compiled Documents or specify custom names. Board Level Annotation is also useful if you are implementing *Device Sheets* in your project since Board Level Annotation is the annotation of the Compiled Documents not the source document, which in the case of Device Sheets, is read-only by default.

Board Level Annotation gives you complete control over the annotation in your project with annotation settings saved in a `*.Annotation` text file, displayed under the `Settings\Annotation Documents` sub-folder in the **Projects Panel**. Altium Designer manages Annotation files automatically.

You can choose to name all of the components in your project, name selected components or name only those components which are undesignated.

To annotate the compiled components in your project through the Schematic Editor:

- Ensure that the components have been annotated at the *Schematic Level* so that the Schematic source data including packaged options for multi-part components is available as input for your Board Level Annotation
- Select **Tools » Board Level Annotate** (**CTRL+L**) which brings up the *Board Level Annotate* dialog. The left hand side of the dialog is for filtering and setting the scope of annotation and the right hand side shows the proposed changes
- Note that the project is compiled every time you perform a Board Level Annotation to ensure the most current design and preferences are used.

Figure 17. The Board Level Annotate dialog is displayed with all of the Schematic Documents in your project.

Filter Options

The left hand side of the *Board Level Annotate* dialog allows you to control the scope of annotation at the Sheet, Channel and Part Level. The columns in the **Filter Options** control do not change.

Schematic Sheet

The **Schematic Sheet** column lists all of the Schematic Documents in your project. A Schematic Document may be listed more than once if your design includes multiple channels.

Channel Name

The **Channel Name** column lists all of the relevant channels in your design. If there are no channels in the design, this column will be populated with the Schematic Sheet name.

Enabled

Tick the check box to include the Schematic Sheet for a specific Channel in this Board Level Annotation. Uncheck the box to exclude this sheet from Board Level Annotation.

Annotation Scope

Choose from the following to set the scope for the parts to be annotated:

- **All** – All parts in the Schematic Sheet will be annotated
- **Ignore Selected Parts** – All parts except those selected will be annotated
- **Only Selected Parts** – Only the parts selected will be annotated

Note: Parts to be excluded or included in Board Level Annotation need to be selected before you open the *Board Level Annotate* dialog.

All On, All Off Buttons

When pressed, the **All On** button ticks the **Enabled** checkbox for all Schematic Sheets in the project, including them in annotation. The **All Off** button disables the Enabled checkbox for all Schematic Sheets in the project, excluding them from annotation.

Proposed Change List

The right hand side of the *Board Level Annotate* dialog allows you to view Schematic Source Components (highlighted in pink), view Calculated Design Data used in the current naming scheme whether this is the default names for compiled components or the applied naming scheme, (highlighted in green), apply a Naming Scheme and view the resultant PCB Component Instance.

Schematic Source Component

The Schematic Source Component section is made up of three columns:

- Hierarchy Path – the path of the Schematic Source, in the format `Filename\Channel`
- Prefix –the alphabetical prefix extracted from the Schematic Level Designator e.g if your Schematic Level Designator is R13, the Prefix is R.

Note: If the component is undesignated, it will have a component icon with a question mark. After you perform your first Board Level Annotation, the icon changes to to show that the component has a designator. If you Reset your designators, the icon will revert to .

- Local Index – the index you have specified following the alphabetical prefix, extracted from the Schematic Level Designator e.g if the Schematic Level Designator is R13, the Local Index is 13.

Calculated Design Data

Upon first opening the Board Level Annotate Dialog, the Calculated Design Data section displays the Room Name column, which corresponds to the default **Annotate Option** selected.

Once you have performed a Board Level Annotation, the columns displayed in the Calculated Design Data represent the keywords selected in your naming scheme for annotation in your **Annotate Options.** These columns are updated dynamically based on your selection. For example, if you select your Naming Scheme to be `$GlobalIndex.$SheetDesignator`, the columns displayed will be Global Index and Sheet Designator.

Naming Scheme

Tick the check box to enable the Naming Scheme for this component. Uncheck the box to disable the Naming Scheme for this component. Note that when this field is unchecked, the PCB Component Instance column can be edited so you can specify a custom designator for your component.

PCB Component Instance

The PCB Component Instance column displays the proposed designator. This field is dictated by either the Naming Scheme selected or a custom value which can only be specified when the Naming Scheme field is unchecked. The custom name can contain any combination of alphanumeric and non-alphanumeric characters.

Annotate Options

The **Annotate Options** allows you to further customize your Annotation using either predefined or custom Naming Schemes.

Predefined Naming Schemes

To apply a predefined naming scheme:

- Click the **Annotate Options** button. The *Board Level Annotation Options* dialog appears
- Select a predefined Naming Scheme from the drop down list
- Once you have selected a Naming Scheme, customize any other options such as Global Index Options or Room Name Options and click **OK**
- Notice that the Calculated Design Data columns are updated to reflect the keywords used in your Naming Scheme.

Custom Naming Schemes

To apply a custom naming scheme:

- Click the **Annotate Options** button. The *Board Level Annotation Options* dialog appears
- Define your own Naming Scheme using valid keywords. You can select any combination of valid keywords in any order to define your own Naming Scheme. You can use any non-alphanumeric character in your Naming Scheme to separate keywords e.g. `_` `*` `.` `@` etc
- Choose from the keywords tabulated below:

Keyword	Definition
$RoomName	Name of the associated Room, as determined by the style chosen in the Room Name Options
$ComponentPrefix	Component Logical Designator prefix (e.g. U for U1)
$ComponentIndex	Component Logical Designator index (e.g. 1 for U1)
$ChannelPrefix	Logical Sheet Symbol Designator
$ChannelIndex	Index you have specified to distinguish between different channels
$ChannelAlpha	Channel Index expressed as an alpha character. This format is only useful if your design contains less than 26 channels in total, or if you are using a hierarchical designator format
$SheetDesignator	Designator assigned to the Sheet Symbol
$SheetNumber	The Sheet Number assigned to the Sheet. If Compiled Sheets have been annotated, this information will be used
$DocumentNumber	The Document Number specified in Document Options
$GlobalIndex	User defined index. You can specify the order, Start Index and/or a suffix in the Global Index Options for each schematic document. These options are displayed in the Board Level Annotation Options dialog. Global Index is calculated for all undesignated components. If you add new components after you have performed a Board Level Annotation, these components will be annotated with a new Global Index and the existing components will retain their Global Index. To recalculate the Global Index for all components, **Reset All** first.

Alternatively, if you wish to specify a custom name for all or a particular component, uncheck the **Apply** box under Naming Scheme column to disable the Naming Scheme for selected components and edit PCB Component Instance column.

Annotate

To complete Board Level Annotation:

- Click on the Annotate drop down and choose whether you want to **Annotate Undesignated**, **Annotate All** or **Annotate Selected**
- The **PCB Component Instance** column is updated with the designator to be annotated to each component

- Click the **Accept Changes (Create ECO)** button. The *Engineering Change Order* dialog appears, allowing you to validate, report and execute the ECO.
- Click **Execute Changes** button and then the **Close** button to execute Board Level Annotation
- Click the **Close** button on the **Board Level Annotate** dialog

Your `*.Annotation` file will be updated and you can view your Board Level Annotation in your Compiled Documents. To complete Board Level Annotation, synchronize your Schematic Documents with your PCB Documents by selecting **Update PCB Document** `Filename` from the **Design** menu.

Reset All

Use the **Reset All** button to reset all of the designators back to the *default names for Compiled Components*. These default names are configured in the *Project Options* dialog accessed through the **Project** menu. Once components have been reset, The Prefix column will display a component icon with a question mark to show that the component is now undesignated.

Back Annotation

Click the **Back Annotate** button to synchronize changes from your PCB design to the Compiled Documents in the Schematic Editor. After clicking the **Back Annotate** button, the *Choose WAS-IS File for Back-Annotation from PCB* dialog appears. Choose your file for Back Annotation.

Back Annotation for Board Level Annotation performs the same way as it does for Schematic Level Annotation. Note that Back Annotation is a legacy tool and it is best practice to use **Design » Update** to push annotation changes from the PCB back to the schematic.

Figure 18 The Annotate Compiled Sheets dialog.

Annotating Compiled Sheets

You can annotate your compiled sheets using the **Tools » Annotate Compiled Sheets** command. This function enables you to uniquely name the Compiled Documents (the physical representation of your design). These values are mapped to the `SheetNumber` special string and are stored in the `*.Annotation` file. This file is displayed under `Settings\Annotation Documents` sub-folder so that annotation information is remembered when you close your project. **Annotate Compiled Sheets** command treats Device Sheets like other sheets in your project and annotates them according to your Annotation options.

Annotating Compiled Sheet Options

Click on the **Annotate Sheet** drop down combo to choose your Compiled Sheet Annotation Options.

Numbering Order

- **Display Order**: The sheets are annotated in the order they are displayed
- **Sheets Hierarchical Structure – Depth First**: The sheets are annotated from the top level into each branch. The top level is annotated first and then the first branch under the top level is annotated completely, the second branch and so on.

Document	Hierarchy Path	Sheet Number
EqualizerTop.SchDoc	EqualizerTop	1
EqualizerChannel.SchDoc	EqualizerTop\1kHz	2
RCNetwork.SchDoc	EqualizerTop\1kHz\Left	3
RCNetwork.SchDoc	EqualizerTop\1kHz\Right	4
EqualizerChannel.SchDoc	EqualizerTop\2kHz	5
RCNetwork.SchDoc	EqualizerTop\2kHz\Left	6
RCNetwork.SchDoc	EqualizerTop\2kHz\Right	7
EqualizerChannel.SchDoc	EqualizerTop\4kHz	8
RCNetwork.SchDoc	EqualizerTop\4kHz\Left	9
RCNetwork.SchDoc	EqualizerTop\4kHz\Right	10

The Navigator view of your project shows the compiled (physical) representation of your sheets. When you annotate the sheets 'depth first', you annotate each branch of the hierarchical structure at a time.

- **Sheets Hierarchical Structure – Breadth First**: The sheets are annotated according to their level in the hierarchy. Top level is annotated first, all second levels are annotated next and so on.

Document	Hierarchy Path	Sheet Number
EqualizerTop.SchDoc	EqualizerTop	1
EqualizerChannel.SchDoc	EqualizerTop\1kHz	2
EqualizerChannel.SchDoc	EqualizerTop\2kHz	3
EqualizerChannel.SchDoc	EqualizerTop\4kHz	4
EqualizerChannel.SchDoc	EqualizerTop\8kHz	5
EqualizerChannel.SchDoc	EqualizerTop\16kHz	6
EqualizerChannel.SchDoc	EqualizerTop\32Hz	7
EqualizerChannel.SchDoc	EqualizerTop\64Hz	8
EqualizerChannel.SchDoc	EqualizerTop\125Hz	9
EqualizerChannel.SchDoc	EqualizerTop\250Hz	10

The Navigator view of your project shows the compiled (physical) representation of your sheets. When you annotate the sheets breadth first', you annotate the sheets based on their position in the hierarchy. For example, the top sheet, `EqualizerTop.SchDoc` is annotated first and then all of the second level sheets are annotated next.

Numbering Method

Choose to **Increase** or **Decrease** the annotation of your compiled sheets based on the **Numbering Order** chosen.

Annotating Compiled Sheets

After selecting your options:

- Click the **Annotate Sheet** button, the **Sheet Number** field will be updated to match your selections
- Click **OK** to accept your changes.

Refer to the section, *Displaying Physical Names in your Compiled Documents* for more information about displaying sheet number parameters in your project.

Custom Annotation of your Compiled Sheets

You can create custom names for your Compiled Sheets by typing directly into the **Sheet Number** field. You can use any combination of alphanumeric or non-alphanumeric characters. After entering your custom names, click **OK** to implement your custom annotation.

Using Compiled Sheet Annotation in your Board Level Annotation

Once you have annotated your Compiled Sheets, use the `$SheetNumber` keyword in your naming scheme when performing a Board Level Annotation to use this information in your annotation. If you have not annotated your compiled sheets, the Schematic Sheet numbering (**Tools » Number Schematic Sheets**) information will be used.

Using Compiled Sheet Annotation in your Project

Once you have annotated your compiled sheets, you can place the `SheetNumber` special string in your project to reference this information.

- Ensure that you have **Convert Special Strings** enabled in **DXP » Preferences » Schematic » Graphical Editing**
- Place a special string where the value `=SheetNumber` to use your Compiled Sheet Annotation values. You can use Special Strings in values of Parameter Properties, Text Strings, Net Labels etc.

For more information on Special Strings, refer to the *Schematic Editor and Object Reference*.

Board Level Annotation and Device Sheets

Device Sheets are portable and can be re-used between designs. In most cases, the names of the components in Device Sheets are limited to the scope of that sheet, and require Board Level Annotation in order to be incorporated into the design in which they are placed.

Board Level Annotation is relevant to Device Sheets due to the fact that different Device Sheets included in one project can contain duplicate designators, resulting in compilation errors. Board Level Annotation can resolve any conflicting naming with the changes saved to a `*.Annotation` file displayed under the `Settings\Annotation Documents` sub-folder.

Default Names for Compiled Components

Default Names are required to be able to distinguish between the different instances of the physical representations of components. These default names are displayed in your Compiled Documents and are used if you have not performed a Board Level Annotation to annotate your compiled (physical) components. When you first launch the *Board Level Annotate* dialog, the default names are populated in the **PCB Component Instance** column.

Default naming of compiled components is also applicable for Multi-Channel designs which reference the same sheet in a project multiple times. This is done by either placing multiple sheet symbols which reference the same sheet in the Schematic Document or by including the **Repeat** keyword in the designator of a sheet symbol, to instantiate a sheet multiple times.

While this makes it easy to repeat circuitry, it also presents a challenge in terms of annotation. In a Multi-Channel design there can only be one logical instance of each component with its own unique designator, no matter how many “copies” of it exists on the PCB.

The **Multi-Channel** tab accessed through **Project » Project Options** ensures that each channel is uniquely annotated with a default name based on Room Naming Styles and Component Designator Format.

Multi-Channel Tab

Rooms are regions that assist in the placement and annotation of components in multi-channel designs. More specifically, a *channel* on the Schematic is an instance of a repeated sheet and on the PCB, each *channel* is represented by a *room.* Once components have been assigned to a room, they move when the room is moved, allowing separate channels to be easily controlled and identified.

Rooms play an important role in channel designations ensuring unique names.

Logical designators are assigned to the components in the Schematic Editor View. Physical designators are assigned to the components when they are placed in the PCB design or when you have performed a Board Level Annotation. In multi-channel designs, the logical designators for repeated channel components may be the same, but each component must have a unique physical designator in the PCB design. This can be accomplished by appending the Room Name to the component name as shown in the **Component Naming** field below.

The **Multi-Channel** tab of the *Options for Project* dialog allows you to specify the room naming style and the component designator naming format for your designs. By controlling the multi-channel designator format in this dialog, you control the mapping from the single logical component in the Schematic Editor View to the multiple physical instances on the PCB. The tab is essentially divided into two areas - **Room Naming** and **Component Naming** (Figure 19).

*Figure 19. The **Multi-Channel** tab allows for flexible default naming formats in Multi-Channel designs.*

Room Naming

Use the **Room Naming Style** drop-down list to define the naming format you require for the rooms in your design. These rooms are created by default when you update the project schematics to the PCB. There are five styles available — two flat and three hierarchical.

Flat room name formats	Hierarchical room name formats
Flat Numeric with Names	Numeric Name Path
Flat Alpha with Names	Alpha Name Path
	Mixed Name Path

Hierarchical room names are formed by concatenating all channelized sheet symbol designators (ChannelPrefix + ChannelIndex) in the relevant channel path hierarchy.

As you select a room naming style from the list, the graphical representation is dynamically updated to reflect the naming convention that will appear in the design. The image below gives an example of a 2x2 channel design (a nested 2 channel design, each of those channels has 2 channels within it). The larger cross-hatch regions represent the 2 upper level channels (or Banks) and the shaded regions within represent the lower level channels (with two sample components shown in each). When the design is compiled, a room is created for each sheet in the design, including each bank and each lower-level channel.

Use the **Level Separator for Paths** field to specify the required character/symbol for separating the path information when using the hierarchical naming styles. There are no restrictions on the character used for the Level Separator; however, a single non-alphanumeric character is easier to read.

Figure 20. For the 2x2 channel design shown in the image, a total of 6 rooms will be created - one for each of the 2 Banks and one for each of the 4 lower level channels.

Component Naming

There are several designator formats available for naming components. You can choose a format or define your own using valid keywords.

Define the Component Naming format by selecting from the **Designator Format** drop-down list. There are eight predefined formats — five flat and three that can be used in a hierarchical context:

Flat Designator Formats
$Component$ChannelAlpha
$Component_$ChannelPrefix$ChannelAlpha
$Component_$ChannelIndex
$Component_$ChannelPrefix$ChannelIndex
$ComponentPrefix_$ChannelIndex_$ComponentIndex
Hierarchical Designator Formats
$Component_$RoomName
$RoomName_$Component
$ComponentPrefix_$RoomName_$ComponentIndex

The Flat Designator Formats name each component designator in a linear progression, starting from the first channel, avoiding the duplication of designators. The Hierarchical Designator Formats include the Room Name in the designator for a component. If the Room Naming style chosen is one of the two possible flat styles, then the style for the component designator will also be flat. However, if a hierarchical style has been chosen for Room Naming, the component designator will also be hierarchical as the path information will be included in the format.

The Room Naming style is only relevant for component naming if the $RoomName string is included in the Designator Format.

Defining your own Designator Format

You can define your own component designator format by typing directly into the **Designator Format** field using valid keywords. Select from any combination of the following keywords to construct the format string:

Keyword	Definition
$RoomName	Name of the associated room, as determined by the style chosen in the Room Naming Style field
$Component	Component Logical Designator (e.g. U1)
$ComponentPrefix	Component Logical Designator Prefix (e.g. U for U1)
$ComponentIndex	Component Logical Designator Index (e.g. 1 for U1)
$ChannelPrefix	Logical Sheet Symbol Designator
$ChannelIndex	Index you have specified to distinguish between different channels
$ChannelAlpha	Channel Index expressed as an alpha character. This format is only useful if your design contains less than 26 channels in total, or if you are using a hierarchical designator format

Displaying Physical Names in your Compiled Documents

Your design is constructed in the **Editor** tab. After you have compiled your project, **Compiled Documents** (physical representations of your design) are visible and can be accessed by clicking on the **Compiled Document tabs,** located along the bottom of the Schematic Document in the design window.

You can specify display preferences for the physical names in the Compiled Documents. Compiled Naming Expansion preferences can by customized by:

- Selecting **DXP » Preferences** command which brings up the *Preferences* dialog
- Navigating to the **Compiler** tab under the **Schematic** folder

- In the **Compiled Names Expansion** control, choosing to expand the compiled (physical) names of Designators, Net Labels, Ports, Sheet Numbers or Document Numbers.
- In the **Compiled Names Expansion** control, choosing which names you would like to be displayed in superscript. Choose to either: **Never display superscript** (expanded names are never displayed), **Always display superscript** (expanded names are always displayed) or **Display superscript if necessary** (expanded names are only displayed if they are different from the source)
- Note: The superscript options are applicable to both the Editor tab and your Compiled Document tabs. In the Editor tab, the compiled names are in superscript and in the Compiled Document tabs, the logical name (the name in the Editor tab) is displayed in superscript.

Figure 21. Display preferences for physical names can be specified in the Compiler tab under the Schematic Folder

You may specify your Compiled Naming Expansion Preferences after you perform Board Level Annotation, remembering to compile your project so that these preferences are displayed in your Compiled Documents.

Compiling the project

You must compile your project in order for any changes made to room and/or component designator formats to take effect. Compile the project by selecting **Project » Compile PCB Project**. When your design is compiled, the Editor tab is shown in the Schematic Editor, however now, there are *Compiled Document tabs* displayed along the bottom of the design window.

Once the design has been compiled, it is transferred to the Schematic Editor in the normal way (**Design » Update PCB**). The transfer process will automatically create a component class for each Schematic sheet in the design, a room for each component class and group the components in each class in their room, ready for placement.

PCB Annotation

Positional Annotation in PCB

A key ingredient of good board design is component layout. In a large design, a components' position on the board may have no relationship to its designator, for example, R1 may end up on the opposite side of the board to R2. To make it easy to locate a component on the board, you can re-assign the designators (re-annotate the board) positionally. To systematically assign designators in the PCB Editor based on their position, use **Tools » Re-annotate** which brings up the *Positional Re-Annotate* dialog seen below (Figure 22).

Figure 22.The Positional Re-Annotate dialog shows a graphical representation of each method.

Components are processed or annotated as spatial "bands" in the order specified in the dialog, meaning that parts positioned within the same band are processed first. The "band" is 100 mil wide and the bottom left of the component's bounding rectangle is searched for within the band. An ASCII text file is generated (`DesignName[Date][Time].WAS`) in the same folder as the PCB design document and automatically opened as the active document after a Re-Annotation is done. The file lists initial and re-annotated designator values. Once a **Re-Annotate** has been performed on the PCB, you would typically pass these changes back to Schematic using the **Design » Update** command.

Note that by default, changes made in the PCB Editor will be pushed to the Annotation File only and ultimately Compiled Documents upon compilation when your perform a **Design » Update.** Uncheck the **Push Component Designator Changes to Annotation File** flag in the **ECO Generation** tab in your **Project Options** to push changes to the source Schematic Document only (Editor view).

Best practice is to have all components matched using *unique IDs (UIDs)*, so that annotation of designators in either the Schematic or PCB document can be carried out and the design can be directly resynchronized at any stage using the **Design » Update** command.

Controlling the Display of the Designator on the PCB

Extended Designator strings in a multi-channel design can be tedious to place in the PCB Editor. You can either choose naming options that result in a short name or display the original, logical component designation instead. For example, C30_CIN1 would display as C30. This would necessitate some other notation being added to the board to indicate the separate channels, such as a box being drawn around each channel on the component overlay.

You can select between Logical and Physical designator display on the PCB in the *Board Options* dialog (**Design » Board Options**). If you choose to display the logical designators for components in a multi-channel design, these will be displayed on the PCB and in any output generated such as prints and Gerber's. The unique physical designators, however, are always used when generating a Bill of Materials.

For more information on the handling of common and distributed nets among channels, naming conventions, and PCB rooms and classes for channels, read *Multi-Channel Design Concepts*.

FPGA Annotation

An FPGA design, like a PCB design requires that each component is uniquely labeled or designated. In an FPGA design, the components are annotated using the standard annotation commands. There are annotation-related processes required in an FPGA design, detailed below.

Back-Annotation of Pin Assignments to the FPGA project

Force Annotate All is ideal when you don't care how the FPGA design is annotated.

Every net in your FPGA design that leaves the device must be allocated to a device pin. For an FPGA project (`*.PrjFpg`), pin assignments are defined in a constraint file. Rather than manually assigning every net to a device pin, it is easier to let the vendor place and route software do this. Any pins (ports) that were not assigned in the constraint file prior to place and route are automatically assigned a physical pin during place and route. Since these assignments are needed before the FPGA design can be linked to the PCB design, and the allocation may well change during PCB layout and routing, the vendor pin assignments provide a good starting point. To import the pin assignments from the place and route tool:

1. Open the constraint file, then select **Design » Import Pin File » Select File** from the menu.
2. Navigate to the appropriate vendor-generated pin file. It will be located in a folder with a name like `MyFPGAProject\ProjectOutputs\ProjectBoard`.
3. After selecting the pin file and clicking **OK**, the *Constraint Editor Preferences* dialog will appear. If you enable an option in the dialog, that constraint information will be extracted from the file (if it is available) and included in your constraint file.
4. Save and close the Constraint file. The design is now ready to be linked to the target PCB.

For more information on adding a constraint file to your FPGA project and importing pin assignments, refer to the application note *Re-targeting the design to the Production Board*.

For more information on linking the FPGA project to the PCB project and transferring design changes back and forth, see the *Linking an FPGA Project to a PCB Project* application note.

Back-Annotation from Vendor Pin Files to the PCB Schematic

If you are not designing the FPGA within Altium Designer, you will still need to manage the pin assignments to ensure the PCB and FPGA designs are in-sync. In the Schematic Editor for your PCB project, the FPGA component can be updated directly from the vendor pin file. Back-Annotation data support includes pin name and electrical type. This feature does not require the FPGA to have been designed in Altium Designer, all popular vendor pin files can be read directly. Right-click on the Schematic symbol for the FPGA and select **Part Actions » Import FPGA Pin File** from the floating context menu.

Figure 23. Import pin allocation information directly from FPGA vendor pin files.

Design Synchronization – Finalizing the Annotation Process

Direct Design Synchronization is the preferred method to keep your Schematic and PCB designators matching unless you do not have access to both the Schematic and the PCB editors.

Design Synchronization compares the components and connectivity of the Schematic directly to the PCB, producing a list of differences. A list of changes required to resolve these differences is generated as an ECO (Engineering Change Order). An ECO file describes the differences between the current design and the desired design and can be executed, updating the target and bringing the design into synchronization.

Forward Synchronization and Back Synchronization

The terms *Forward Synchronization* and *Back Synchronization* are specific ways of describing the direction which annotation and design changes are transferred during the synchronization of data.

Visualizing a design flow that starts with and is driven by the Schematic, *Forward Synchronization* is the process of updating changes made in the Schematic Editor *forward* to the PCB.

Back Synchronization is the process of updating changes made in the PCB *backwards* to the Schematic Editor.

Forward Synchronization

There are four reasons why you would synchronize data from the Schematic to the PCB:

1. A new component is added in the Schematic Editor and is required in the PCB layout
2. You have Annotated your Schematic design for the first time or since your last design synchronization
3. In your multi-channel design, you have changed your Project Options to modify your physical (PCB) naming style
4. You have done a Board Level Annotation for the first time or since your last design synchronization.

To Synchronize your Schematic Design forward to the PCB Design:

Choose from one of the following methods to synchronize your Schematic Design forward to your PCB Design:

1. Select the **Design** menu in the Schematic Editor and choose the target PCB Document to update

- After launching this command, the source Schematic Documents are compiled and if any differences exist between these and the target PCB Document, the *Engineering Change Order* dialog appears with a list of modifications required to synchronize the PCB with the Schematic Design
- Execute changes to synchronize your design

2. Select the **Design** menu in the PCB Editor and choose to **Import Changes** from the active project, which imports changes *from* the Schematic Documents *to* the PCB document.

Back Synchronization

Back Synchronization is done when you have annotated or changed your PCB design and you want to update the Schematic design.

To Synchronize your PCB Design back to the Schematic Design:

Choose from one of the following methods to synchronize your PCB Design back to your Schematic Design:

1. Select the **Design** menu in the PCB Editor and choose to **Update Schematics** in the active project. By default, the **Push Component Designator Changes to Annotation File** flag in the **ECO Generation** tab in your **Project Options** is checked so changes made in the PCB Editor will be pushed to the Annotation File only and ultimately Compiled Documents upon compilation. Uncheck this flag to push changes to the source Schematic Document only (Editor view)
2. From the Schematic Editor, select **Tools » Annotate Schematics** and click the **Back Annotate** button in the *Annotate* dialog. Choose the `WAS-IS` file generated when re-annotating designators in the PCB environment. This is a legacy tool and the preferred method of design synchronization is the **Design » Update Schematics** command
3. From the Schematic Editor, select **Tools » Board Level Annotate** and click the **Back Annotate** button in the *Board Level Annotate* dialog. Choose the `WAS-IS` file generated when re-annotating designators in the PCB environment. This is a legacy tool and the preferred method of design synchronization is the **Design » Update Schematics** command
4. From the Schematic Editor, select the **Tools » Back Annotate Schematics** command. Choose the `WAS-IS` file generated when re-annotating designators in the PCB environment. This is a legacy tool and the preferred method of design synchronization is the **Design » Update Schematics** command.

> **Back Annotate** synchronizes annotation changes made in the PCB Editor with the Schematic design. This feature is useful when it is not possible to have the PCB and Schematic Editors open at the same time. For example, when the PCB and the Schematic are designed by different people in different locations.

Traditional Methods of Design Synchronization

Altium Designer supports the traditional intermediate (netlist and WAS/IS) file approach for Design Synchronization. Forward Synchronization of annotation data can be done through the use of a netlist file, whilst Back Synchronization can be done through the use of a WAS/IS file (listing what each designator WAS, and what it now IS). The preferred method for synchronizing your design is Direct Design Synchronization.

Component Linking with Unique IDs

If you have Re-Annotated your design, the Schematic component designators or the compiled component designators will no longer match the PCB component designators, so synchronization is required to successfully close off the design.

Rather than relying on the designator itself as the key field that relates a Schematic symbol to its equivalent PCB footprint, Altium Designer can maintain design synchronization through Unique IDentifier (UID) system. The UID is a system-generated value that uniquely identifies the source component and matches each Schematic component to the corresponding PCB component.

When a component is placed on a schematic sheet it is automatically assigned an UID. The first time component information is transferred from the source Schematic documents to a blank PCB, the UID information from each schematic component is assigned to the corresponding PCB component.

Refactoring allows you to convert *Device Sheets* to Schematic Sheets and vice versa while maintaining the Unique ID of the sheet and its components. In addition, you can refactor (or move) subcircuits to other schematic sheets in the current project, maintaining the Unique ID of the subcircuit. Access this command through the **Edit** menu or by right-clicking on either the Sheet Symbol or the sub circuit and choosing **Refactor**.

Altium Designer's synchronization feature, initiated by launching the **Design » Update** command uses these UIDs to match each Schematic component to its PCB equivalent.

Design updates/changes can then be implemented using Engineering Change Orders (ECOs). An ECO lists all modifications required to implement changes to one or more design documents, in order to satisfy the synchronization action requested.

ECOs are used to affect design updates in a variety of situations, such as:

1. SCH to PCB design updates
2. Performing Annotation updates to Schematic component designators and compiled component designators
3. Implementing updates to parameters using the Parameter Manager
4. Updating parameter information with information stored in source libraries or a company database.

Whenever you compare the Schematic and PCB (such as when you select **Design » Update**) Altium Designer first matches components that share the same UID. When components are detected that do not share a UID, you are alerted and the application offers to attempt to match by designator. Until you have assigned a matching UID to both the Schematic and the PCB, you will continue to get this message.

Unique IDs and their correlation are managed in the *Edit Component Links* dialog. Select **Project » Component Links** to open this dialog. Note that the dialog can only be opened when a PCB document is active as UID changes are always applied to the PCB rather than the Schematic. You can use the *Edit Component Links* dialog at any stage during the design to view the linking between the components to verify that components between documents are correctly matched, as well as to assign matching UIDs to components that are currently unmatched.

If you are planning on re-annotating either the Schematic or the PCB then it is essential that you make sure that the UIDs are matching first, since once you change all the designators on the schematic or PCB, the UID is then the only piece of information that can be used to link the schematic component to its PCB equivalent.

For a complete discussion on finding and resolving differences between the Schematic and the PCB, refer to the article *Finding Differences and Synchronizing Designs*.

Revision History

Date	Version No.	Revision
05-Sep-2006	1.0	New document release
17-Jan-2008	2.0	Updated for Altium Designer 6.8 – Information for Board Level Annotation and new dialog screenshots
25-Jan-2008	2.1	Updated for Altium Designer 6.9 – Changes to the way Global Index is calculated and new feature, Refactoring.
19-Mar-2008	2.2	Updated Page Size to A4.
16-Mar-2011	-	Updated template.

Software, hardware, documentation and related materials:

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